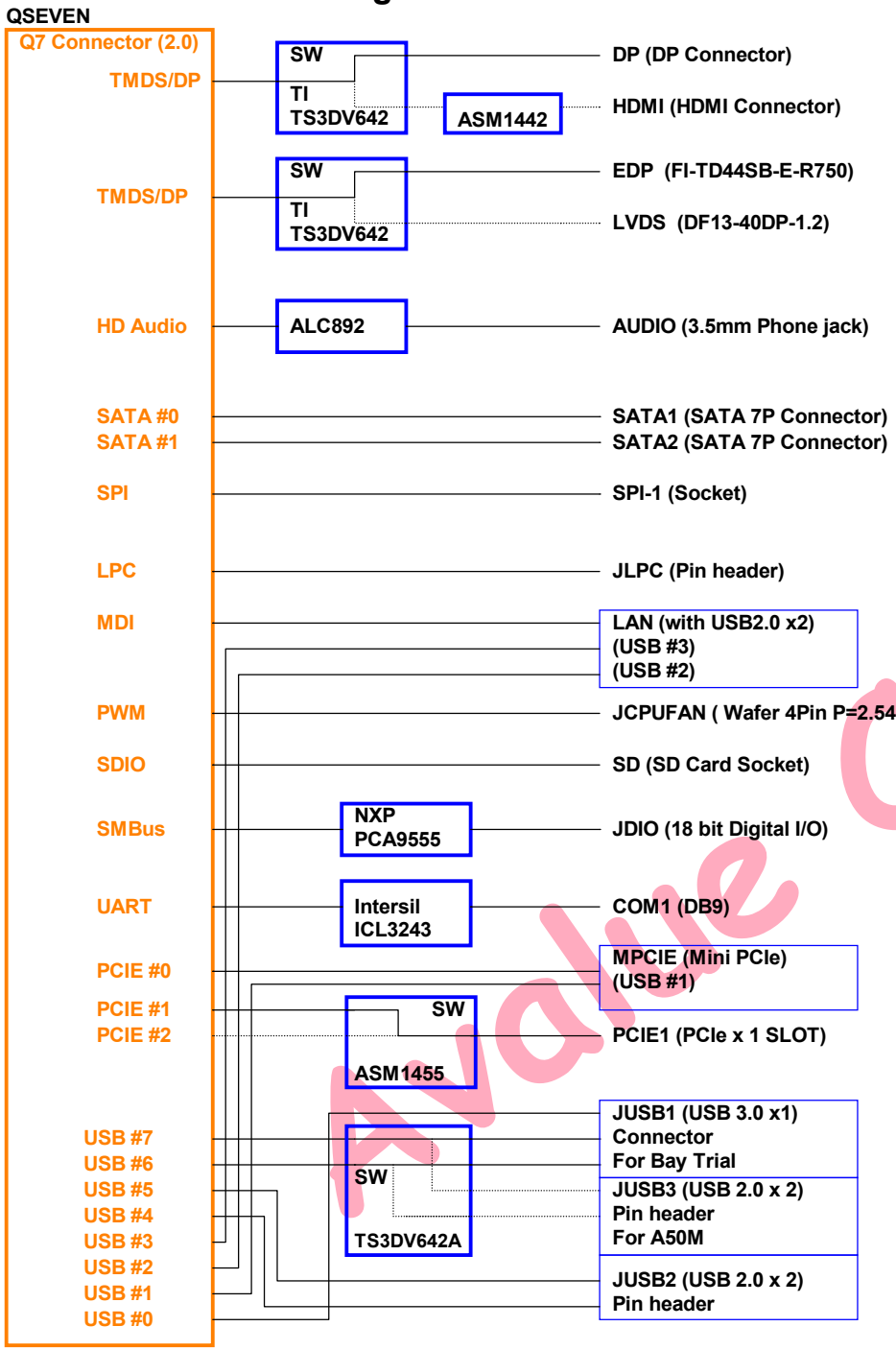
EEV-Q702 Block diagram



Cover Sheet:

#PCB1
PCB
E1907Q70202RO-W1

#SMT1
SMT
E9695Q70202R

#DIP1
DIP
E9697Q70202R

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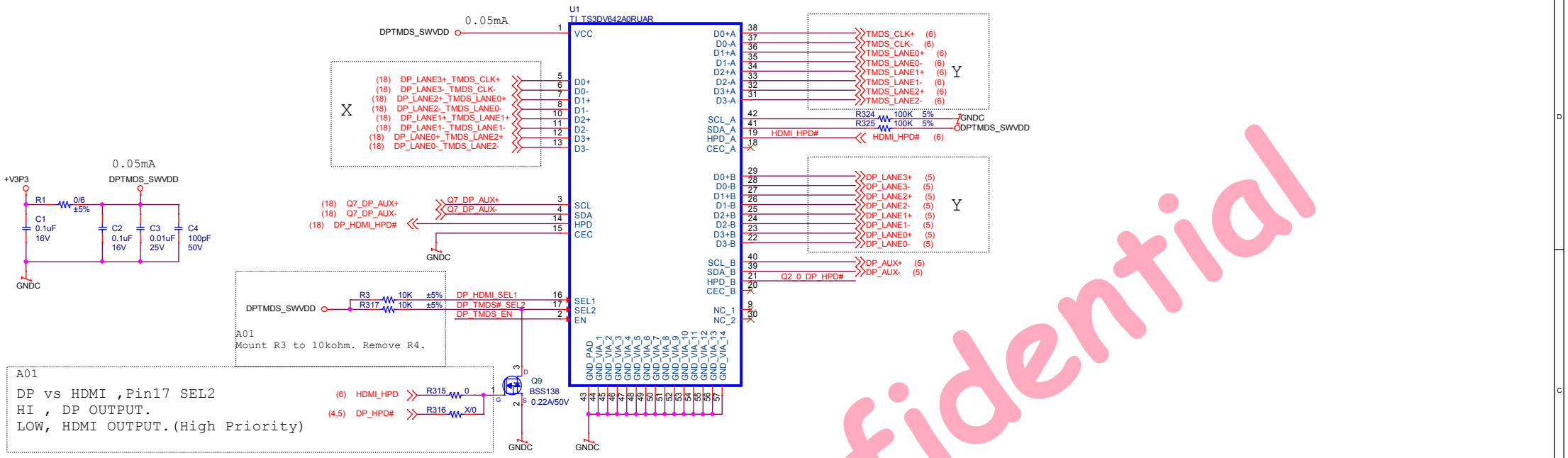
Project Name	Module Number	Rev
EEV-Q702	<Module no.>	?

Size	Title	Rev
A3	Cover Sheet / Block Diagram	A1

Date: Thursday, June 05, 2014 Sheet 1 of 23



EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0– to D0+A/D0–A ON. All the other channels Hi-Z.
H	L	H	D0+/D0– to D0+B/D0–B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

Use all channel.

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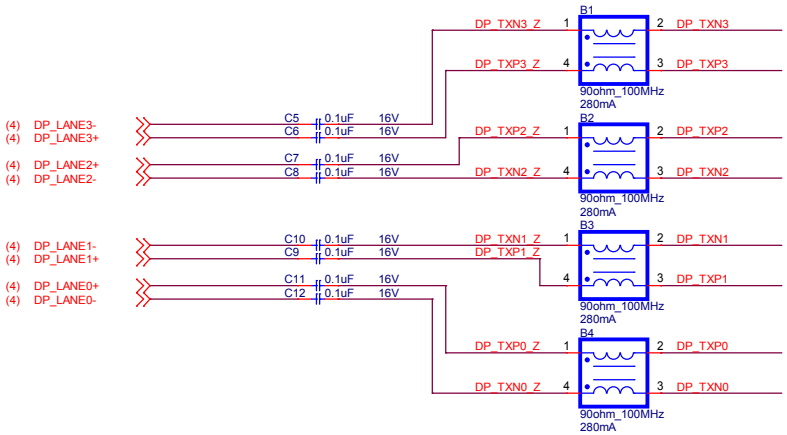
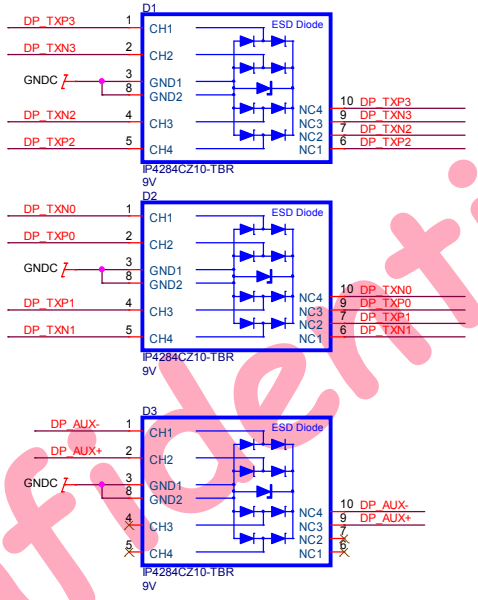
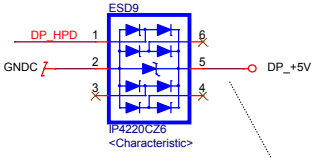
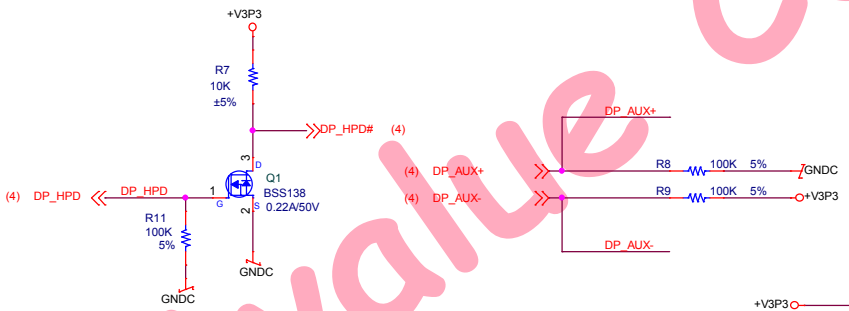
Project Name: EEV-Q702	Module Number: <Module no.>	Rev: ?
Size: A3	Title: DP_TMDS_SWITCH	Rev: A1
Date: Thursday, June 05, 2014	Sheet 4 of 23	

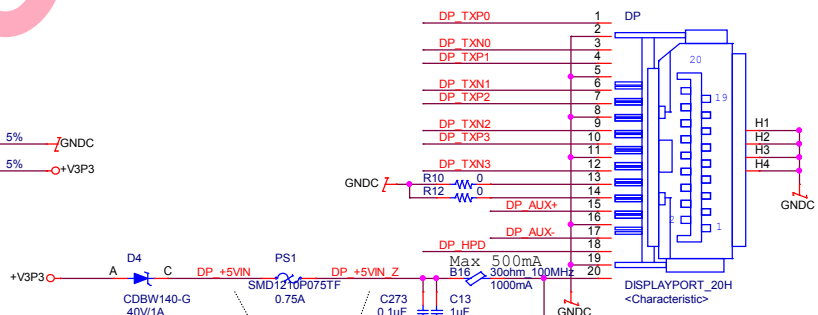






A0 -> A01
Changed to 3.3V level.
Net name unchange.





Trace width 20mils

A0 -> A01
Changed to 3.3V level.
Net name unchange.

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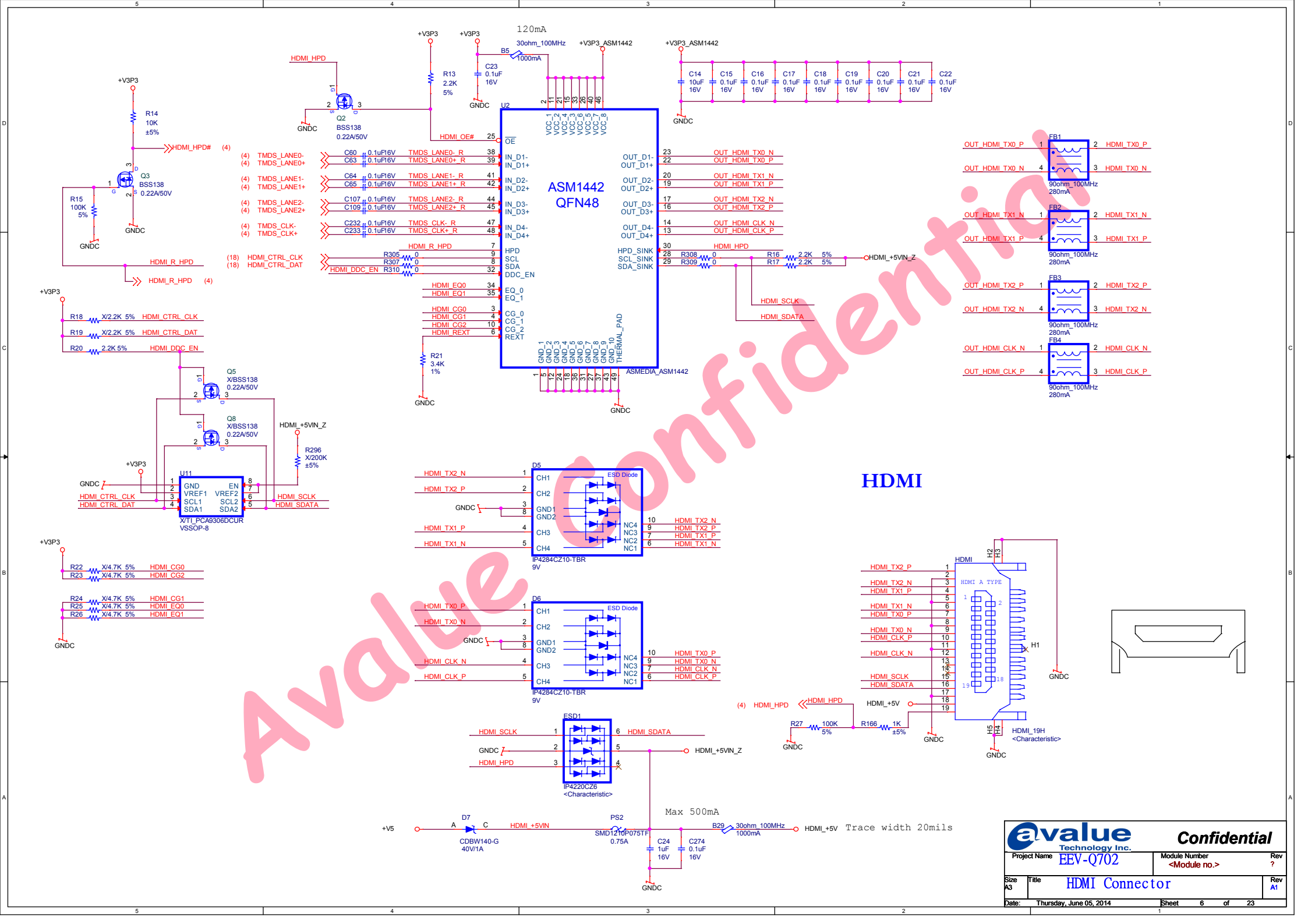
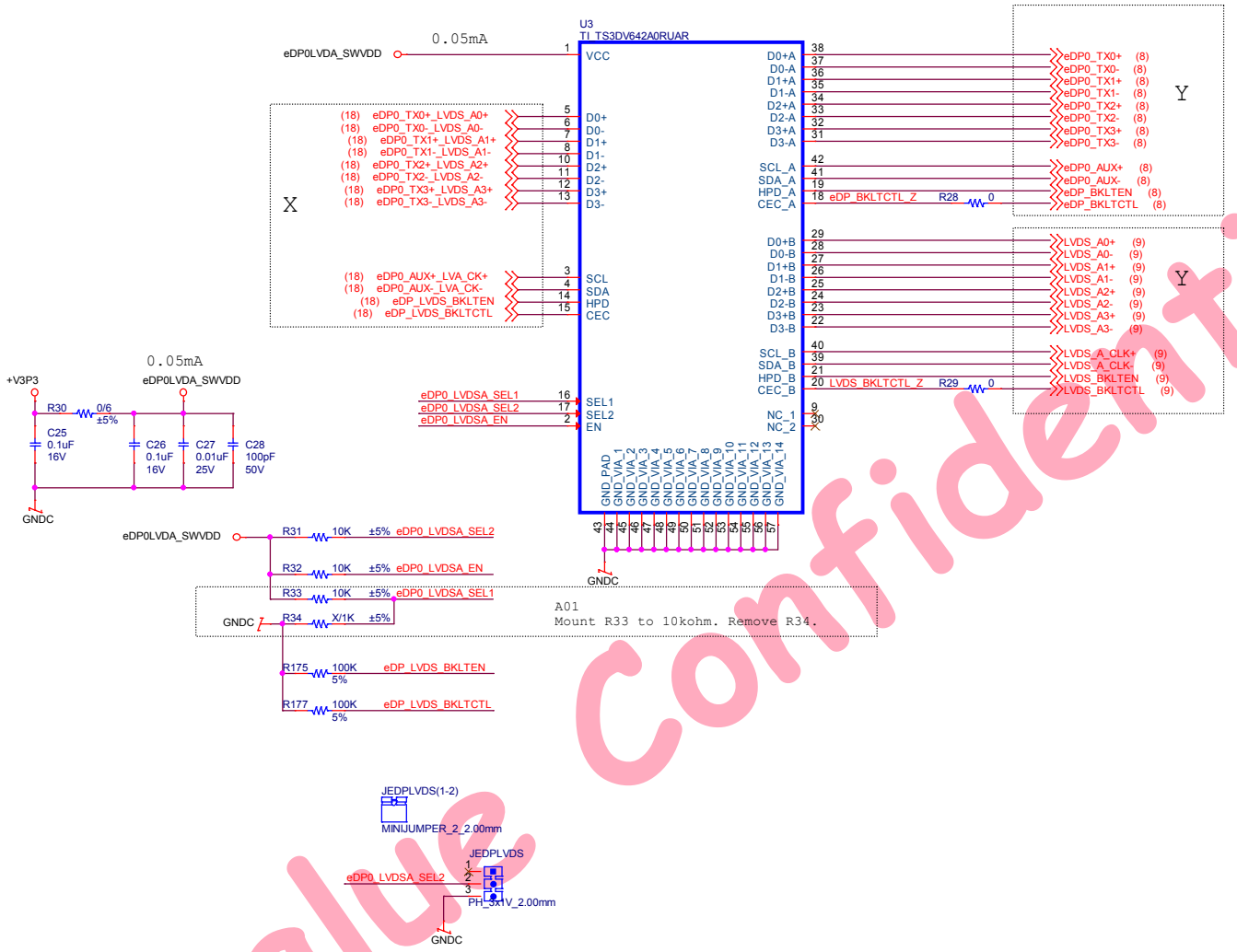
Project Name: EEV-Q702		Module Number: <Module no.>	Rev: ?
Size: A3	Title: DP Connector		Rev: A1
Date: Thursday, June 05, 2014		Sheet 5 of 23	


HDMI
ASM1442
QFN48
ASMEDIA_ASM1442
IP4284CZ10-TBR
9V
ESD Diode
IP4220CZ6
<Characteristic>
X/TI_PCA9306DCUR
VSSOP-8
CDBW140-G
40V/1A
SMD1210P075TF
0.75A
HDMI_19H
<Characteristic>
120mA
Max 500mA
Trace width 20mils
Avalue Confidential
avalue Technology Inc.
Confidential
Project Name EEV-Q702
Module Number <Module no.>
Rev ?
Size A3
Title HDMI Connector
Rev A1
Date: Thursday, June 05, 2014
Sheet 6 of 23



JEDPLVDS SELECTION
eDP VS LVDS
SHORT 1-2 : HI , LVDS A port OUTPUT.(default)
SHORT 2-3 : LOW, eDP 0 port OUTPUT.

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0– to D0+A/D0–A ON. All the other channels Hi-Z.
H	L	H	D0+/D0– to D0+B/D0–B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

USE D0 switch to DA or DB

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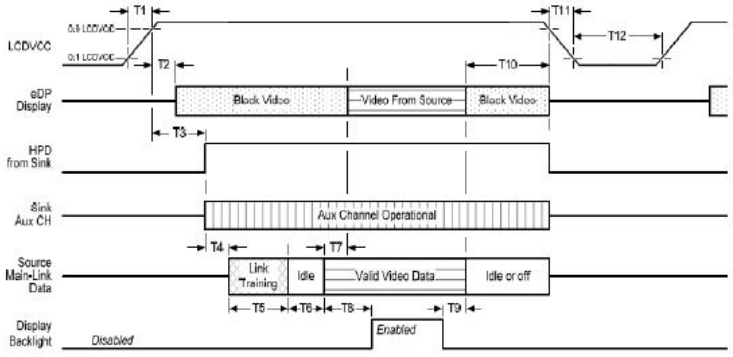
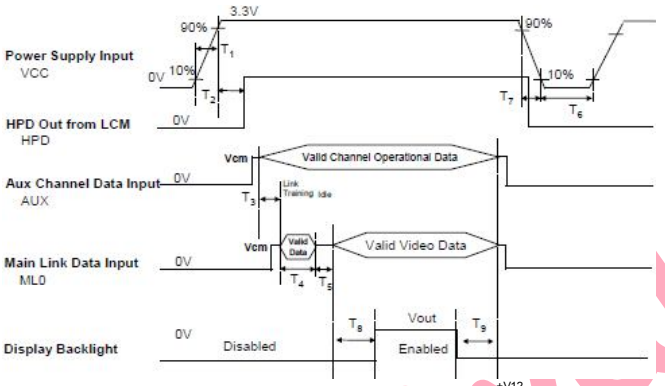
Project Name: EEV-Q702	Module Number: <Module no.>	Rev: ?
Size: A3	Title: eDP_LVDS_SWITCH	Rev: A1
Date: Thursday, June 05, 2014	Sheet 7 of 23	

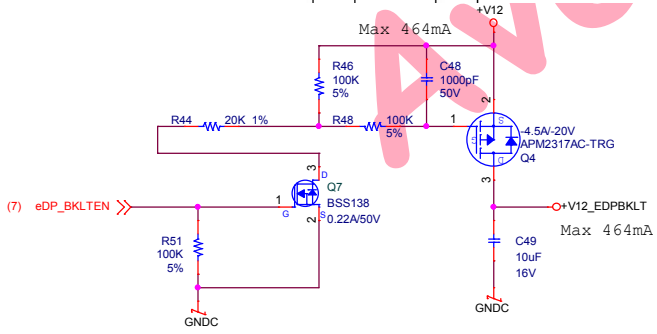
eDP Connector

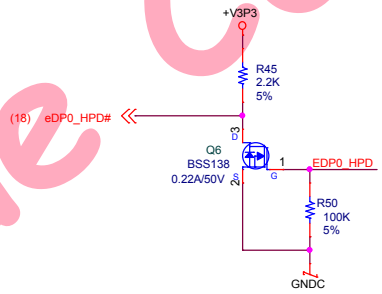
AUO B140HAN01.1 eDP LCD
LCD_VDD (3.3V)
IDD (433mA)
Inrush Current (1500mA)
Backlight power (5V~21V)
Backlight current (333mA / typ:12V)
LVD_VCC input -> HPD -> AUX -> Link Data -> BKLT 12V input -> BKLT EN

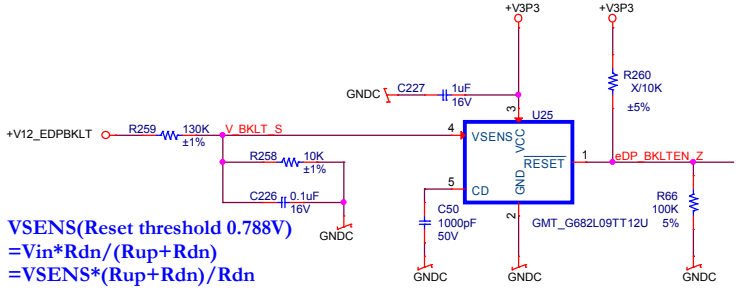


LG LP129QE1 eDP LCD
LCD_VDD (3.3V)
IDD (1200mA)
Inrush Current (2000mA)
Backlight power (Max 42V)
Backlight current (464mA / typ:12V)
LVD_VCC input -> HPD -> AUX -> Link Data -> BKLT 12V input (No enable control)



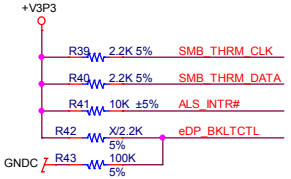


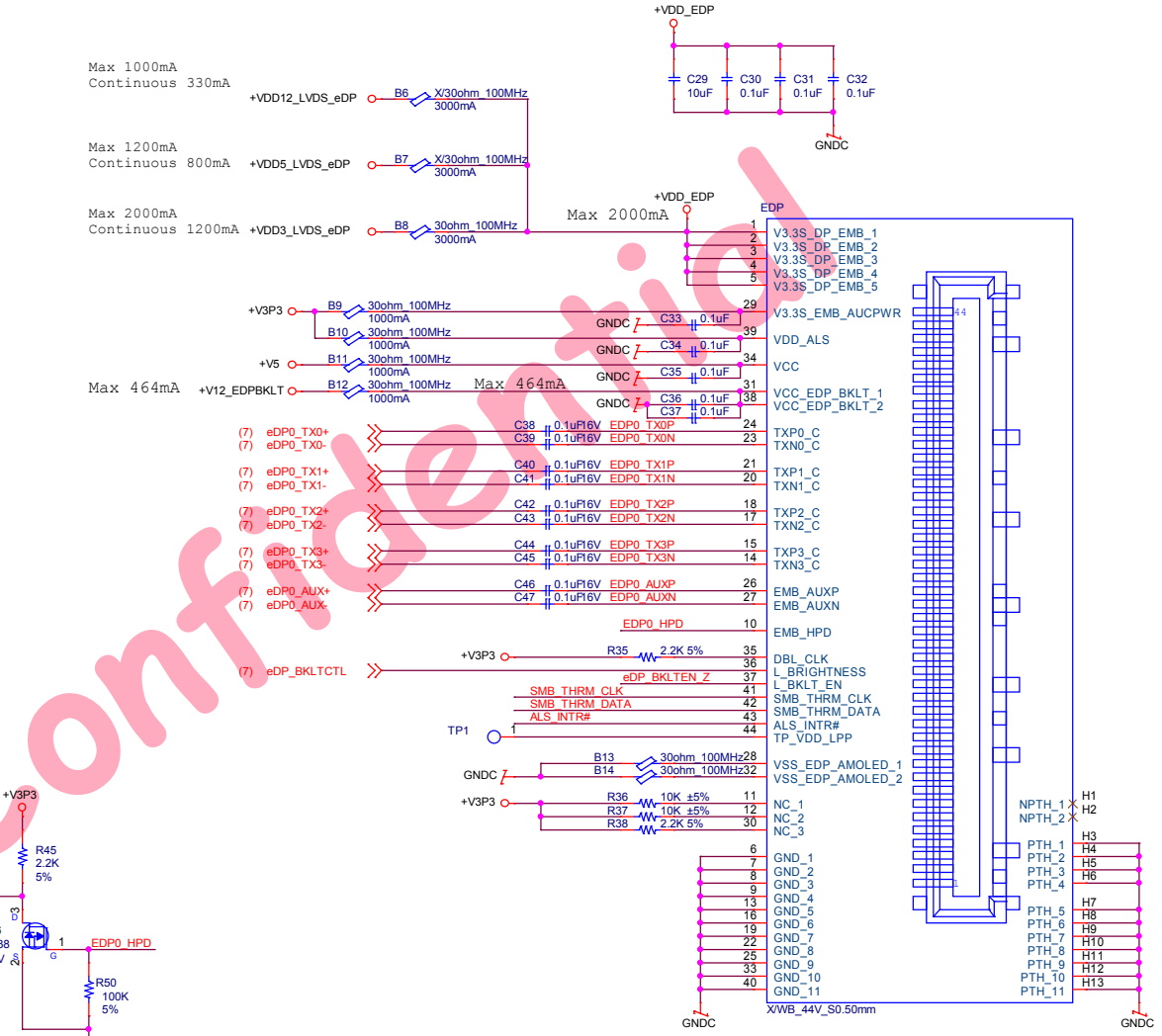




VSENS(Reset threshold 0.788V)
=Vin*Rdn/(Rup+Rdn)
=VSENS*(Rup+Rdn)/Rdn
=11V

tRP (ms)=2.7 × CD (nF) at VCC=3.3V
=~2.7ms





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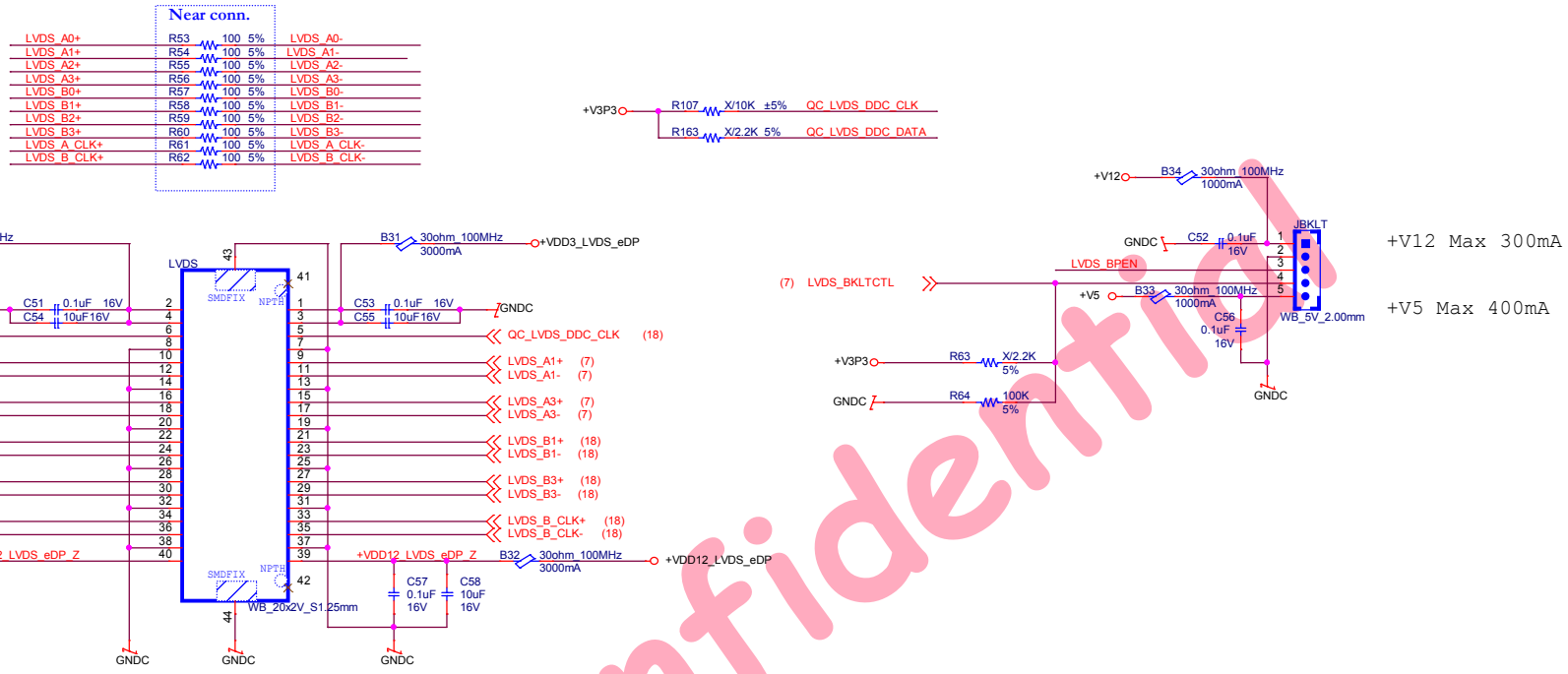
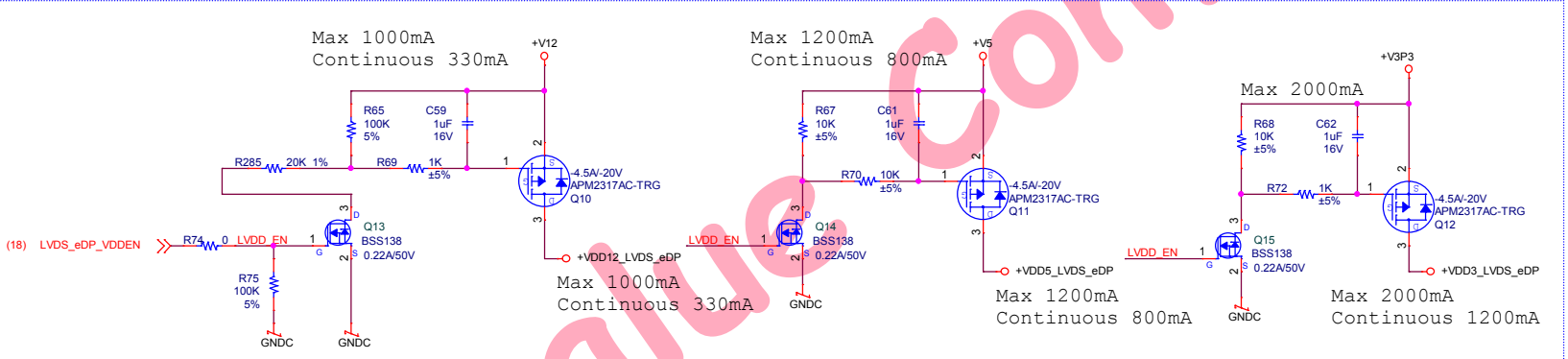
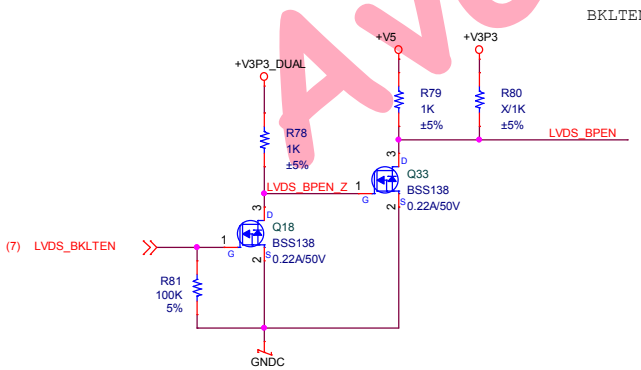
Project Name: EEV-Q702		Module Number: <Module no.>	Rev: ?
Size: A3	Title: eDP Connector		Rev: A1
Date: Thursday, June 05, 2014		Sheet 8 of 23	

LVDS







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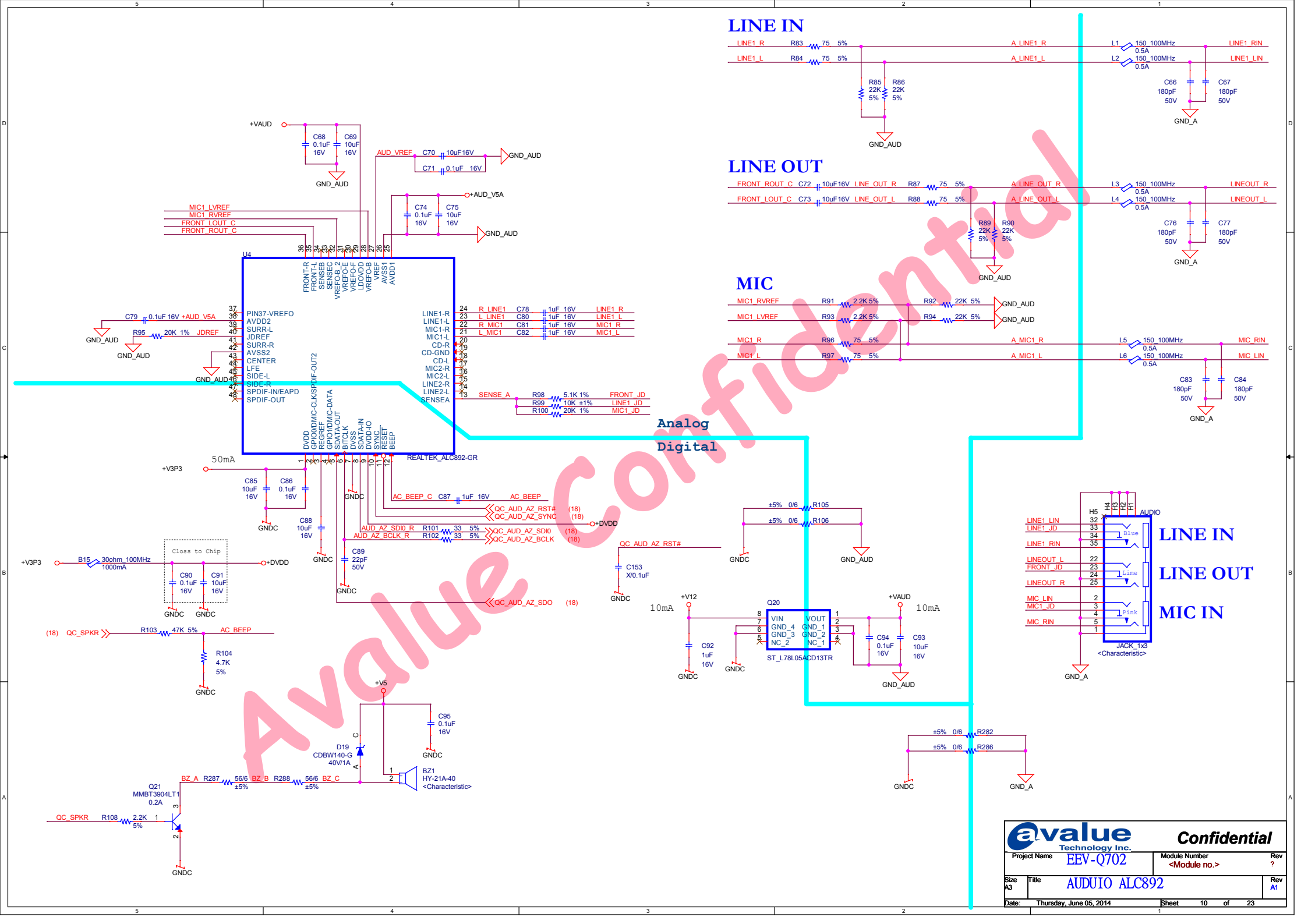
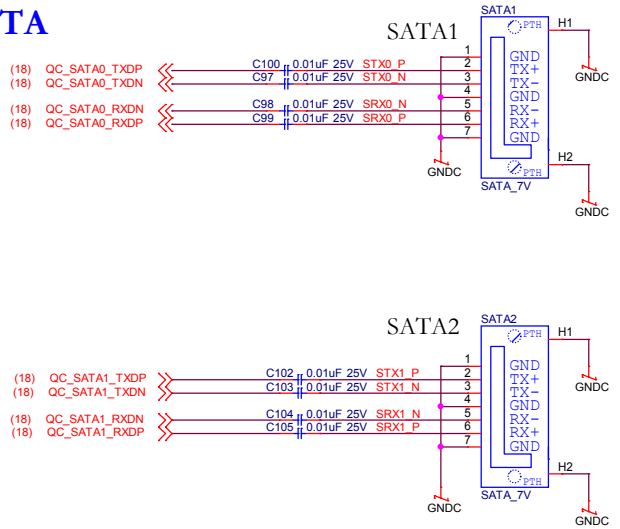
Project Name EEV-Q702		Module Number <Module no.>	Rev ?
Size A3	Title LVDS Connector		Rev A1
Date: Thursday, June 05, 2014		Sheet 9 of 23	


LINE IN
LINE1_R
LINE1_L
R83 75 5%
R84 75 5%
A_LINE1_R
A_LINE1_L
L1 150_100MHz 0.5A
L2 150_100MHz 0.5A
LINE1_RIN
LINE1_LIN
R85 22K 5%
R86 22K 5%
C66 180pF 50V
C67 180pF 50V
GND_AUD
GND_A
LINE OUT
FRONT_ROUT_C
LINE_OUT_R
LINE_OUT_L
C72 10uF16V
C73 10uF16V
R87 75 5%
R88 75 5%
A_LINE_OUT_R
A_LINE_OUT_L
L3 150_100MHz 0.5A
L4 150_100MHz 0.5A
LINEOUT_R
LINEOUT_L
R89 22K 5%
R90 22K 5%
C76 180pF 50V
C77 180pF 50V
MIC
MIC1_RVREF
MIC1_LVREF
R91 2.2K 5%
R92 22K 5%
R93 2.2K 5%
R94 22K 5%
MIC1_R
MIC1_L
R96 75 5%
R97 75 5%
A_MIC1_R
A_MIC1_L
L5 150_100MHz 0.5A
L6 150_100MHz 0.5A
MIC_RIN
MIC_LIN
C83 180pF 50V
C84 180pF 50V
+VAUD
C68 0.1uF 16V
C69 10uF 16V
AUD_VREF
C70 10uF16V
C71 0.1uF 16V
+AUD_V5A
C74 0.1uF 16V
C75 10uF 16V
MIC1_LVREF
MIC1_RVREF
FRONT_LOUT_C
FRONT_ROUT_C
U4
REALTEK_ALC892-GR
PIN37-VREFO
AVDD2
SURR-L
JDREF
SURR-R
AVSS2
CENTER
LFE
SIDE-L
SIDE-R
SPDIF-IN/EAPD
SPDIF-OUT
LINE1-R
LINE1-L
MIC1-R
MIC1-L
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
SENSEA
R_LINE1 C78 1uF 16V
L_LINE1 C80 1uF 16V
R_MIC1 C81 1uF 16V
L_MIC1 C82 1uF 16V
SENSE_A
R98 5.1K 1%
R99 10K ±1%
R100 20K 1%
FRONT_JD
LINE1_JD
MIC1_JD
C79 0.1uF 16V +AUD_V5A
R95 20K 1% JDREF
Analog
Digital
50mA
+V3P3
C85 10uF 16V
C86 0.1uF 16V
C88 10uF 16V
C89 22pF 50V
AC_BEEP_C C87 1uF 16V AC_BEEP
QC_AUD_AZ_RST# (18)
QC_AUD_AZ_SYNC (18)
QC_AUD_AZ_SDI0 (18)
QC_AUD_AZ_BCLK (18)
QC_AUD_AZ_SDO (18)
AUD_AZ_SDI0_R R101 33 5%
AUD_AZ_BCLK_R R102 33 5%
+DVDD
B15 30ohm 100MHz 1000mA
Close to Chip
C90 0.1uF 16V
C91 10uF 16V
(18) QC_SPKR
R103 47K 5%
R104 4.7K 5%
AC_BEEP
+V5
C95 0.1uF 16V
D19 CDBW140-G 40V/1A
BZ1 HY-21A-40 <Characteristic>
BZ_A R287 56/6 ±5%
BZ_B R288 56/6 ±5%
BZ_C
Q21 MMBT3904LT1 0.2A
QC_SPKR R108 2.2K 5%
±5% 0/6 R105
±5% 0/6 R106
QC_AUD_AZ_RST#
C153 X/0.1uF
+V12
10mA
Q20
ST_L78L05ACD13TR
VIN VOUT GND_4 GND_1 GND_3 GND_2 NC_2 NC_1
C92 1uF 16V
C94 0.1uF 16V
C93 10uF 16V
+VAUD
10mA
±5% 0/6 R282
±5% 0/6 R286
AUDIO
H5 H4 H3 H2 H1
LINE1_LIN
LINE1_JD
LINE1_RIN
LINEOUT_L
FRONT_JD
LINEOUT_R
MIC_LIN
MIC1_JD
MIC_RIN
Blue
Lime
Pink
JACK_1x3 <Characteristic>
LINE IN
LINE OUT
MIC IN
GNDC
GND_AUD
GND_A
Avalue Confidential
avalue Technology Inc.
Confidential
Project Name EEV-Q702
Module Number <Module no.>
Rev ?
Size A3
Title AUDUIO ALC892
Rev A1
Date: Thursday, June 05, 2014
Sheet 10 of 23

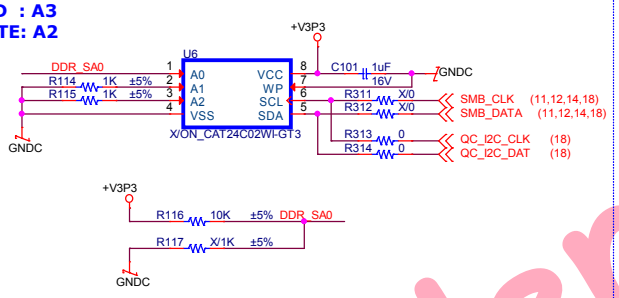
SATA



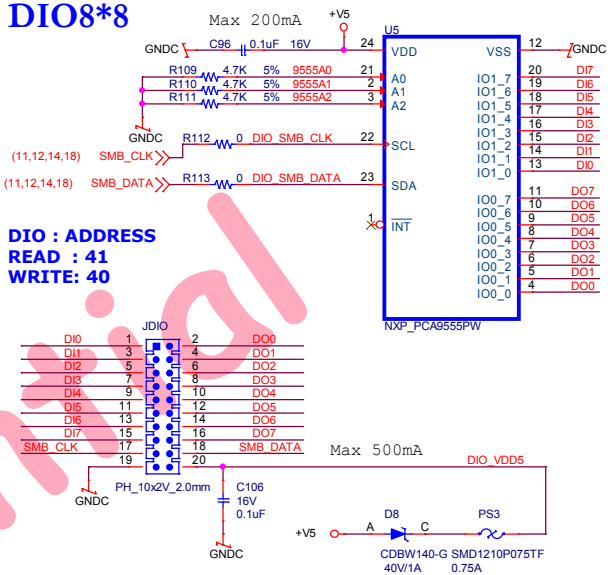
SPD

1	0	1	0	A_2	A_1	A_0	R/$\overline{W}$

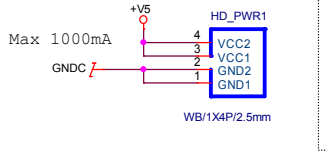
DDR3 SPD: ADDRESS
READ : A3
WRITE: A2

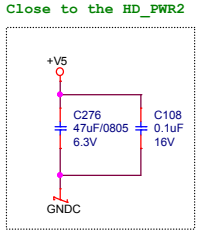


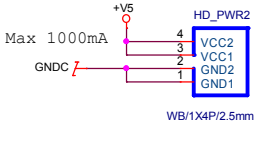
DIO8*8

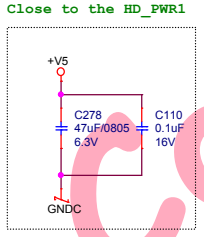


DIO : ADDRESS
READ : 41
WRITE: 40

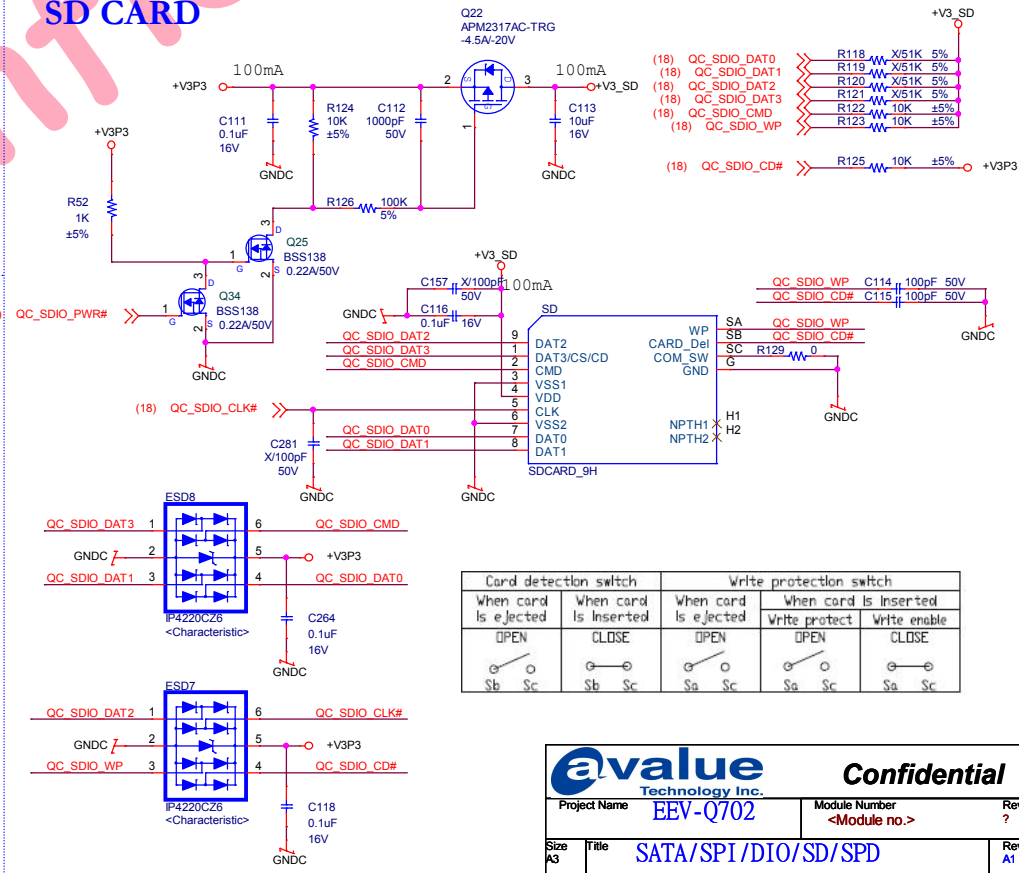






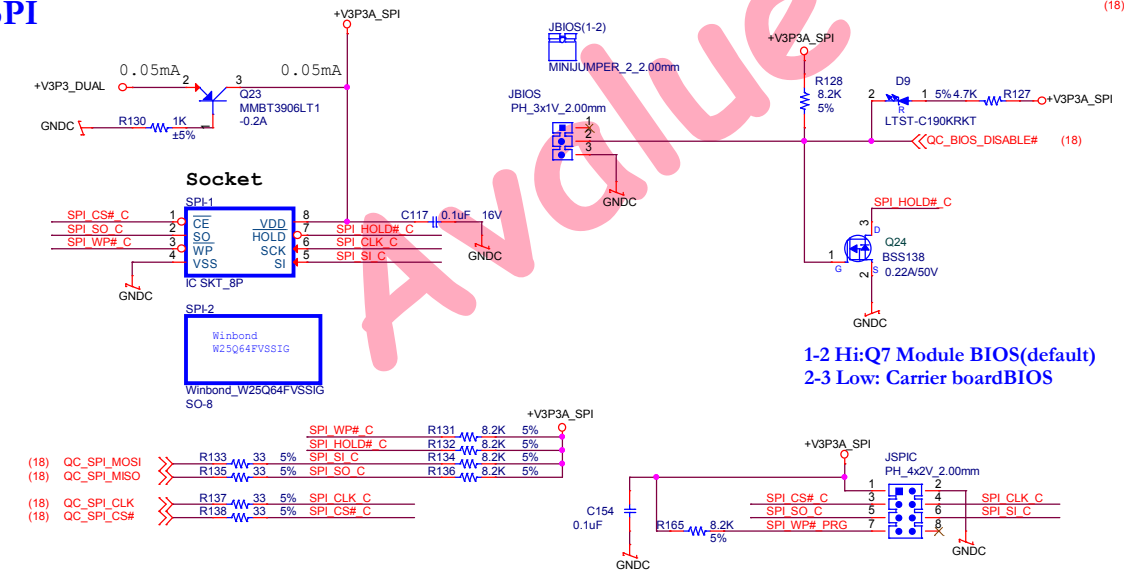


SD CARD



Card detection switch		Write protection switch		
When card is ejected	When card is Inserted	When card is ejected	When card is Inserted	
			Write protect	Write enable
OPEN	CLOSE	OPEN	OPEN	CLOSE
Sb Sc	Sb Sc	Sa Sc	Sa Sc	Sa Sc

SPI



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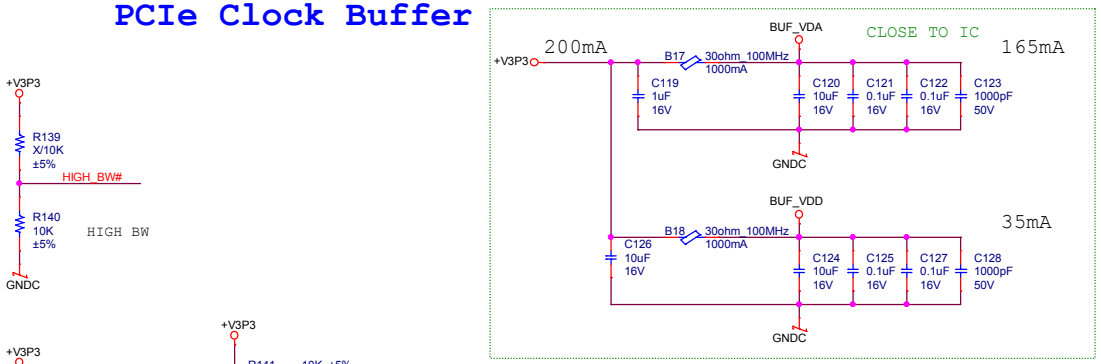
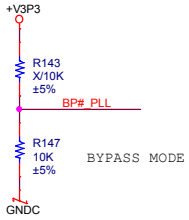
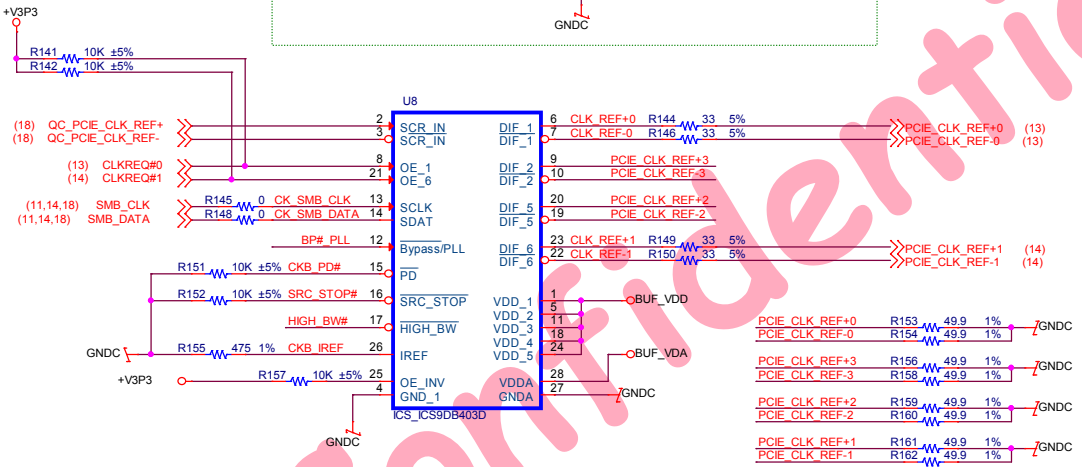
Project Name	EEV-Q702	Module Number	<Module no.>
			Rev ?
Size A3	Title SATA/SPI/DIO/SD/SPD		Rev A1
Date: Thursday, June 05, 2014		Sheet 11 of 23	

PCIe Clock Buffer

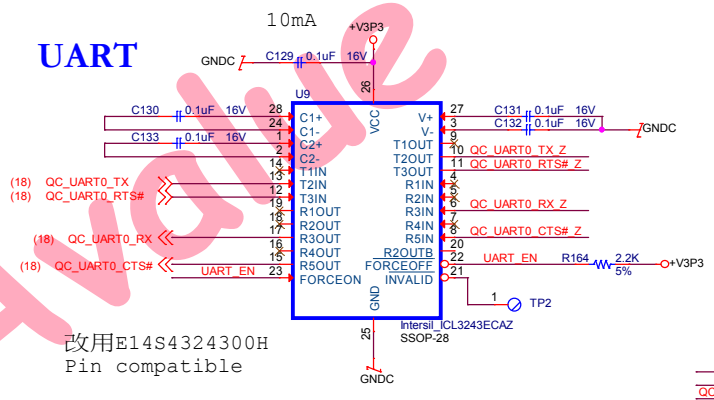




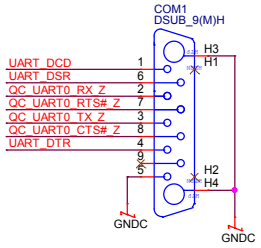
When OE_INV = 1
OE1#=Low active.
OE6#=Low active.
SRC_STOP=High active.
PD=High active.

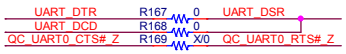


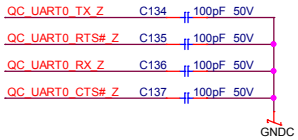
UART



改用E14S4324300H
Pin compatible







While the normal PC hardware might well run with just Tx, Rx and Ground connected, most driver software will wait forever for one of the handshaking lines to go to the correct level. Depending on the signal state it might sometimes work, other times it might not. The reliable solution is to loop back the handshake lines if they are not used.

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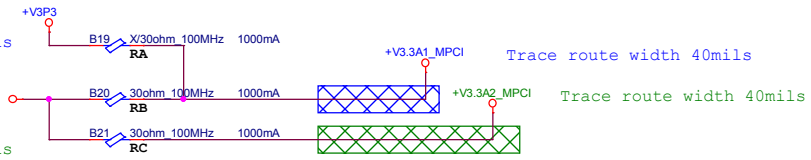
Project Name	Module Number	Rev
EEV-Q702	<Module no.>	?

Size	Title	Rev
A3	PCIE CLOCK BUFFER / UART	A1

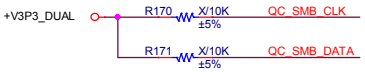
Date: Thursday, June 05, 2014 Sheet 12 of 23

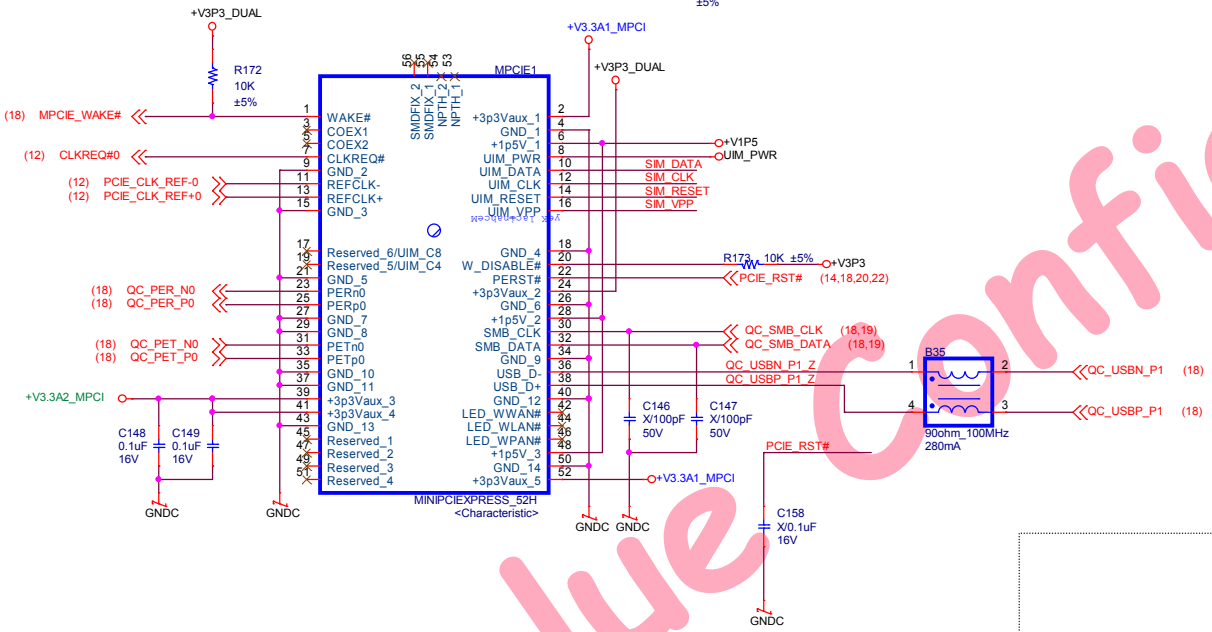
1000mA
Trace route width 40mils

2750mA
Trace route width 80mils

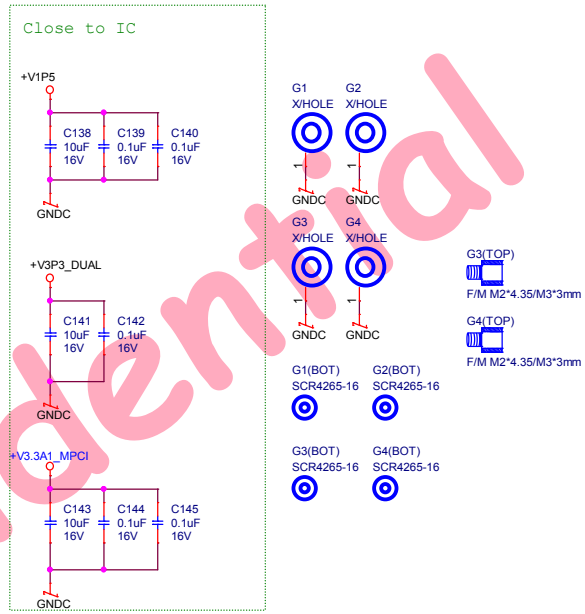


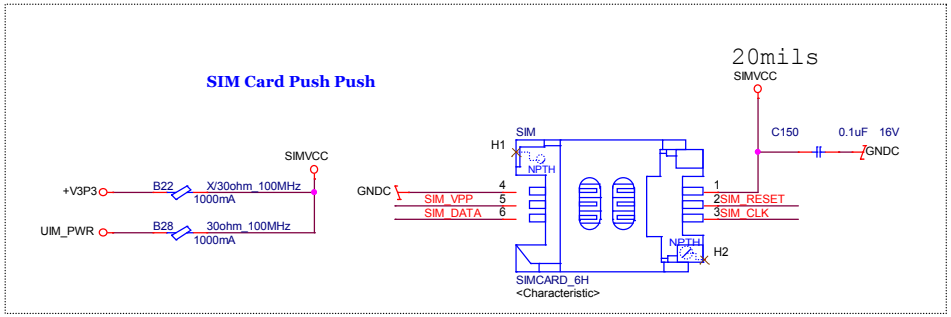
	RA	RB	RC
Mini PCI-E Ver 1.0	O	X	X
Mini PCI-E Ver 1.2	X	O	O





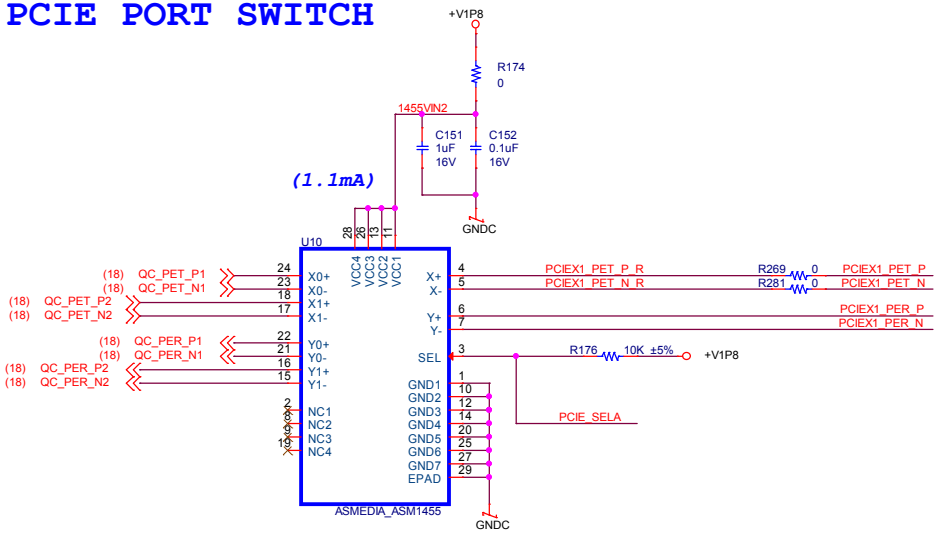
Power Rail	Voltage Tolerance	D0-D2, $D3_{hot}$ Power[1]		$D3_{cold}$ Power[2,3]	
		Peak (max) mA	Normal (max) mA	Peak (max) mA	Normal (max) mA
3.3Vaux	±9%	2,750	1,100	2,750 (wake enabled)	250 (wake enabled) 5 (no wake enabled)
+1.5V	±5%	500	375	N/A	N/A





avalue Technology Inc.	Confidential	
Project Name EEV-Q702	Module Number <Module no.>	Rev ?
Size A3	Title MINI PCIE Connector	Rev A1
Date: Thursday, June 05, 2014	Sheet 13 of 23	

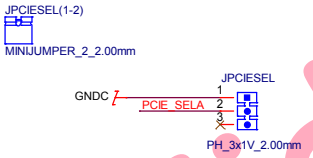
PCIE PORT SWITCH



SEL	Descriptions
L	(X±, Y±) to (X0±, Y0±)
H	(X±, Y±) to (X1±, Y1±)

JPCIESEL Set Table

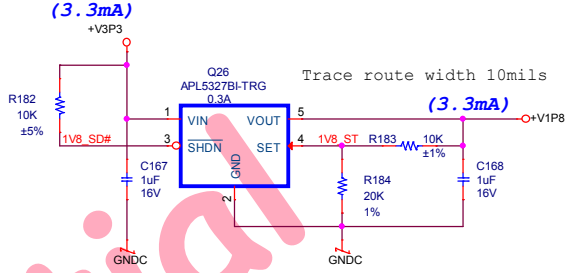
PCIE_SELA		PCIE PORT	
SHORT 1-2		PCIE 1	Default
SHORT 2-3	X	PCIE 2	
X	X	X	



+V1P8 POWER

Trace route width 10mils

(3.3mA)



LDO:VCC3P3 to VCC1P8 - 1.1mA

Vout=1.2[1+(Rup/Rdn)]

=1.8V

When Rdn=20k. Vout=1.8V

Rdn=19.1K. Vout=1.82V

Rdn recommended value is in the range of 100 to100k.

PCI SIG

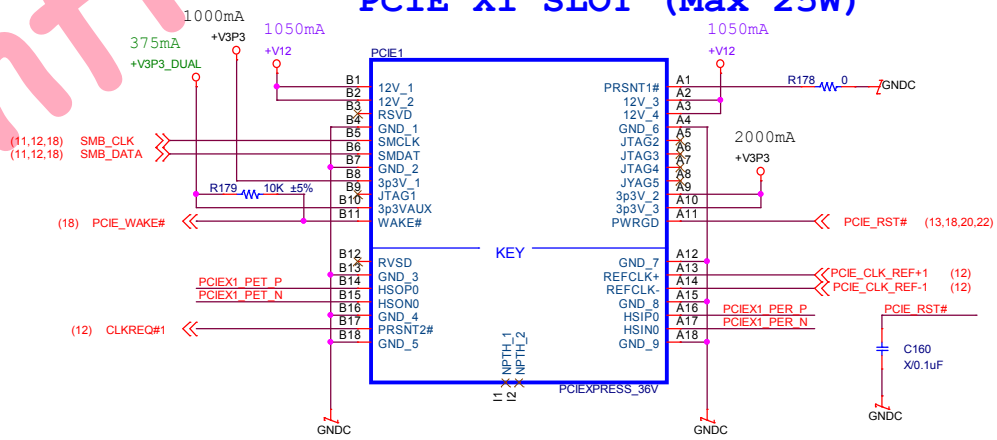
PCI EXPRESS

Power Delivery

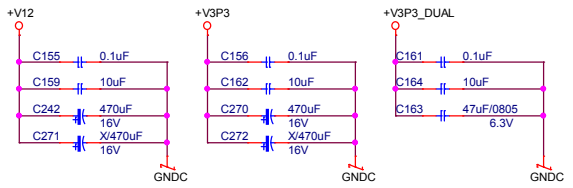
Power Rail	10W slot	25W slot	75W slot
+3.3V ±9%	3A max	3A max	3A max
+12V ±8%	0.5A max	2.1A max	5.5A max
+3.3Vaux ±9%	375mA max	375mA max	375mA max

- Capacitive load rules:
  - ✓ +12V rail: 300µF @ 10W; 1000µF @ 25W; 2000µF @ 75W
  - ✓ +3.3V rail: 1000µF
  - ✓ +3.3Vaux rail: 150µF

PCIE X1 SLOT (Max 25W)



Closed to Connector



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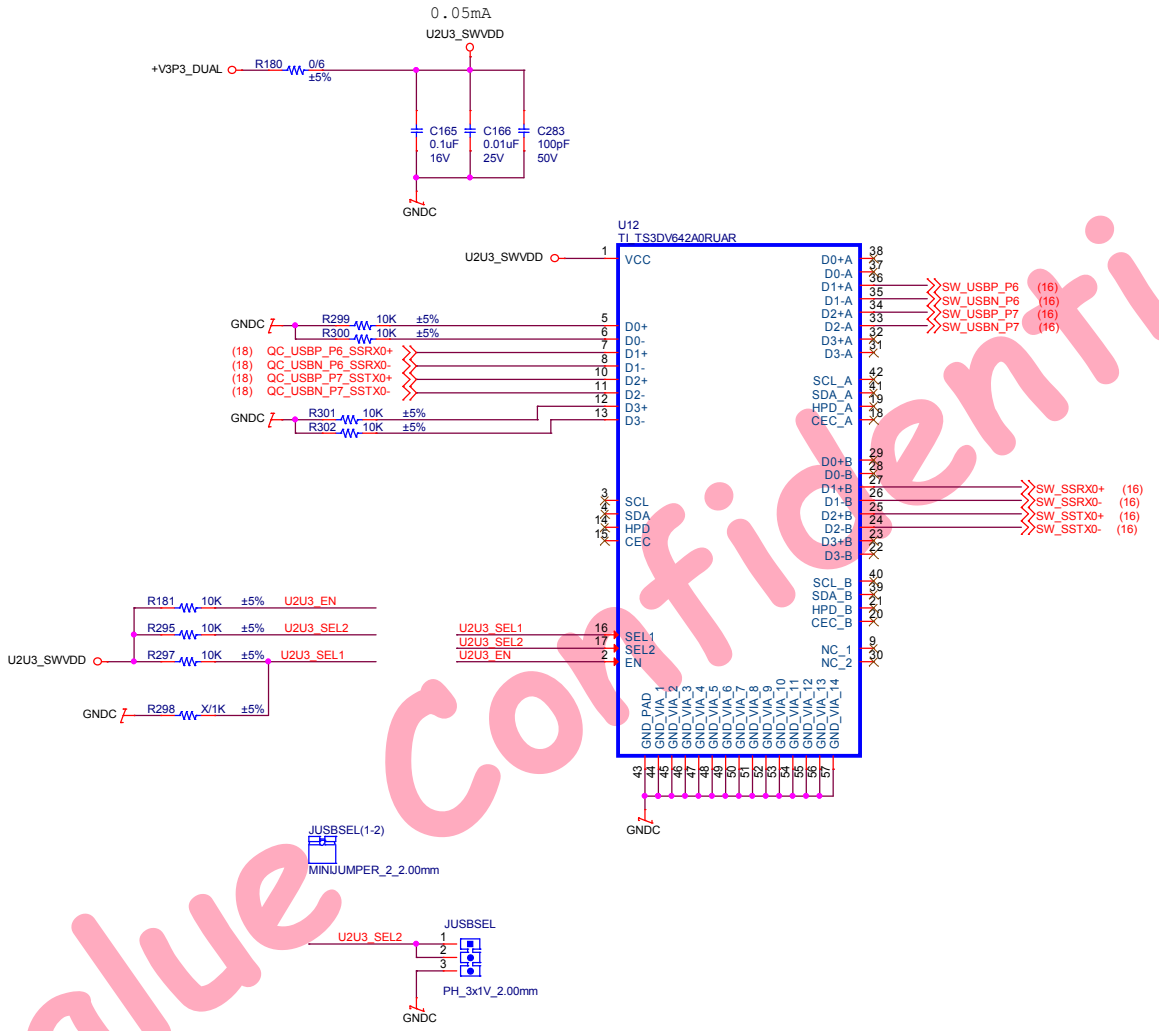
Project Name EEV-Q702		Module Number <Module no.>	Rev ?
Size A3	Title PCIE SWITCH / PCIEx1 SLOT		Rev A1
Date: Thursday, June 05, 2014		Sheet 14 of 23	

USB 2.0 / 3.0 Switch



JUSBSEL1 SELECTION
SHORT1-2: Port 6,7 to B(USB 3.0 , default) or
SHORT2-3: Port 6,7 to A(USB 2.0)

EN	SEL1	SEL2	FUNCTION
L	X	X	Switch Disabled. All Channel Hi-Z.
H	L	L	D0+/D0– to D0+A/D0–A ON. All the other channels Hi-Z.
H	L	H	D0+/D0– to D0+B/D0–B ON. All the other channels Hi-Z.
H	H	L	Channel A Enabled. Channel B Hi-Z.
H	H	H	Channel B Enabled. Channel A Hi-Z.

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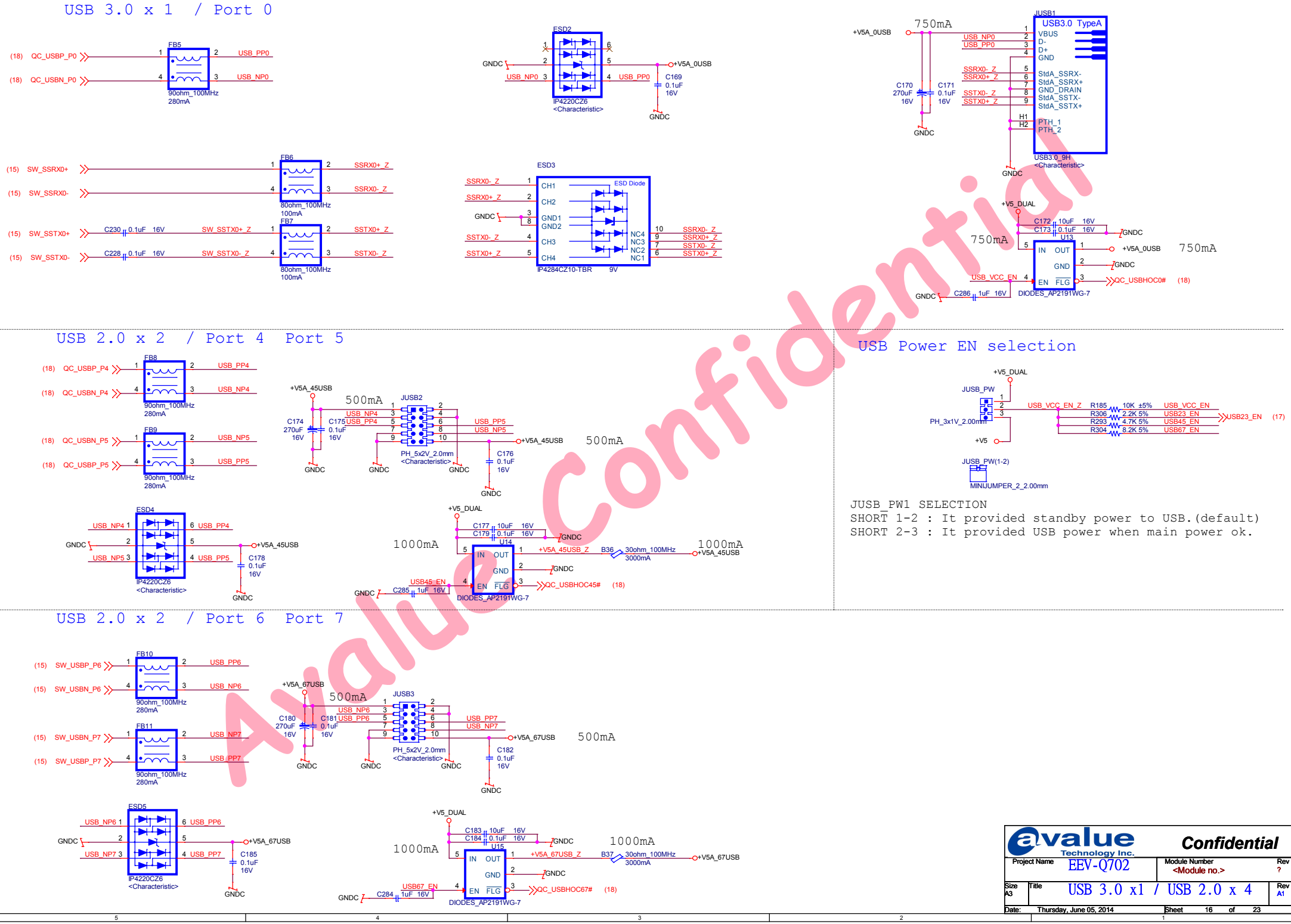
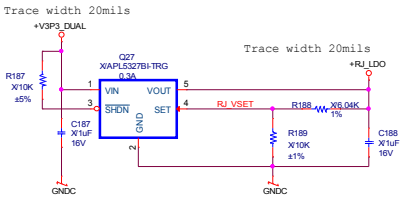
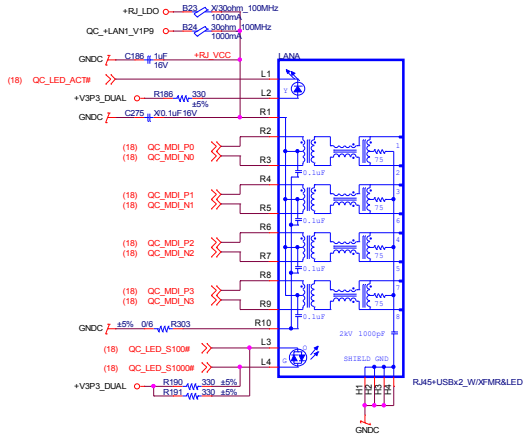
Project Name: EEV-Q702	Module Number: <Module no.>	Rev: ?
Size: A3	Title: USB 2.0 / 3.0 Switch	Rev: A1
Date: Thursday, June 05, 2014	Sheet 15 of 23	

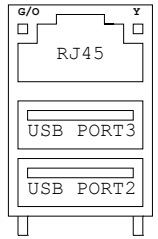

USB 3.0 x 1 / Port 0
FB5
(18) QC_USBP_P0
(18) QC_USBN_P0
USB_PP0
USB_NP0
90ohm_100MHz
280mA
ESD2
GNDC
USB_NP0
USB_PP0
+V5A_0USB
C169
0.1uF
16V
IP4220CZ6
<Characteristic>
750mA
+V5A_0USB
C170
270uF
16V
C171
0.1uF
16V
USB1
USB3.0 TypeA
VBUS
D-
D+
GND
StdA_SSRX-
StdA_SSRX+
GND_DRAIN
StdA_SSTX-
StdA_SSTX+
PTH_1
PTH_2
USB3.0_9H
<Characteristic>
FB6
FB7
(15) SW_SSRX0+
(15) SW_SSRX0-
(15) SW_SSTX0+
(15) SW_SSTX0-
C230 0.1uF 16V
C228 0.1uF 16V
SW_SSTX0+_Z
SW_SSTX0-_Z
SSRX0+_Z
SSRX0-_Z
SSTX0+_Z
SSTX0-_Z
80ohm_100MHz
100mA
ESD3
ESD Diode
CH1
CH2
GND1
GND2
CH3
CH4
NC4
NC3
NC2
NC1
IP4284CZ10-TBR
9V
+V5_DUAL
C172 10uF 16V
C173 0.1uF 16V
U13
IN
OUT
GND
EN
FLG
+V5A_0USB
750mA
USB_VCC_EN
QC_USBHOC0#
(18)
C286 1uF 16V
DIODES_AP2191WG-7
USB 2.0 x 2 / Port 4 Port 5
FB8
FB9
(18) QC_USBP_P4
(18) QC_USBN_P4
(18) QC_USBN_P5
(18) QC_USBP_P5
USB_PP4
USB_NP4
USB_NP5
USB_PP5
90ohm_100MHz
280mA
+V5A_45USB
500mA
C174
270uF
16V
C175
0.1uF
16V
JUSB2
PH_5x2V_2.0mm
<Characteristic>
C176
0.1uF
16V
ESD4
IP4220CZ6
<Characteristic>
C178
0.1uF
16V
+V5_DUAL
C177 10uF 16V
C179 0.1uF 16V
U14
1000mA
+V5A_45USB_Z
B36
30ohm_100MHz
3000mA
USB45_EN
C285 1uF 16V
QC_USBHOC45#
(18)
USB Power EN selection
JUSB_PW
PH_3x1V_2.00mm
USB_VCC_EN_Z
R185 10K ±5% USB_VCC_EN
R306 2.2K 5% USB23_EN
R293 4.7K 5% USB45_EN
R304 8.2K 5% USB67_EN
USB23_EN
(17)
+V5
JUSB_PW(1-2)
MINIJUMPER_2_2.00mm
JUSB_PW1 SELECTION
SHORT 1-2 : It provided standby power to USB.(default)
SHORT 2-3 : It provided USB power when main power ok.
USB 2.0 x 2 / Port 6 Port 7
FB10
FB11
(15) SW_USBP_P6
(15) SW_USBN_P6
(15) SW_USBN_P7
(15) SW_USBP_P7
USB_PP6
USB_NP6
USB_NP7
USB_PP7
90ohm_100MHz
280mA
+V5A_67USB
500mA
C180
270uF
16V
C181
0.1uF
16V
JUSB3
PH_5x2V_2.0mm
<Characteristic>
C182
0.1uF
16V
ESD5
IP4220CZ6
<Characteristic>
C185
0.1uF
16V
C183 10uF 16V
C184 0.1uF 16V
U15
1000mA
+V5A_67USB_Z
B37
30ohm_100MHz
3000mA
USB67_EN
C284 1uF 16V
QC_USBHOC67#
(18)
DIODES_AP2191WG-7
Avalue Confidential
avalue Technology Inc.
Confidential
Project Name EEV-Q702
Module Number <Module no.>
Rev ?
Size A3
Title USB 3.0 x1 / USB 2.0 x 4
Rev A1
Date: Thursday, June 05, 2014
Sheet 16 of 23

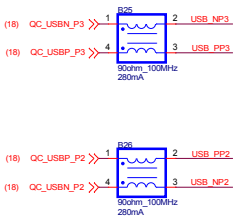
USB 2.0 x 2 / Port 2 Port 3 with RJ45

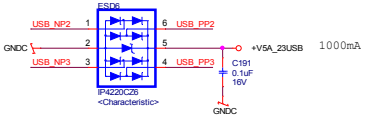


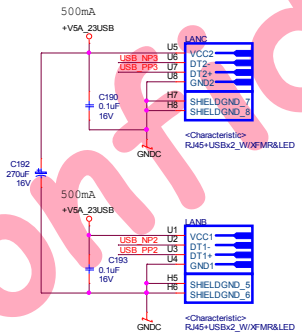
Vout=1.2[1+(Rup/Rdn)]
=1.92V
When Rup=6.04k. Vout=1.92V

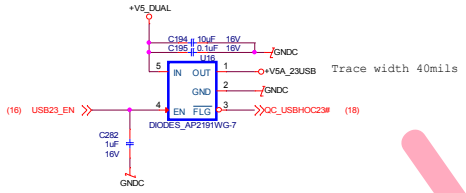












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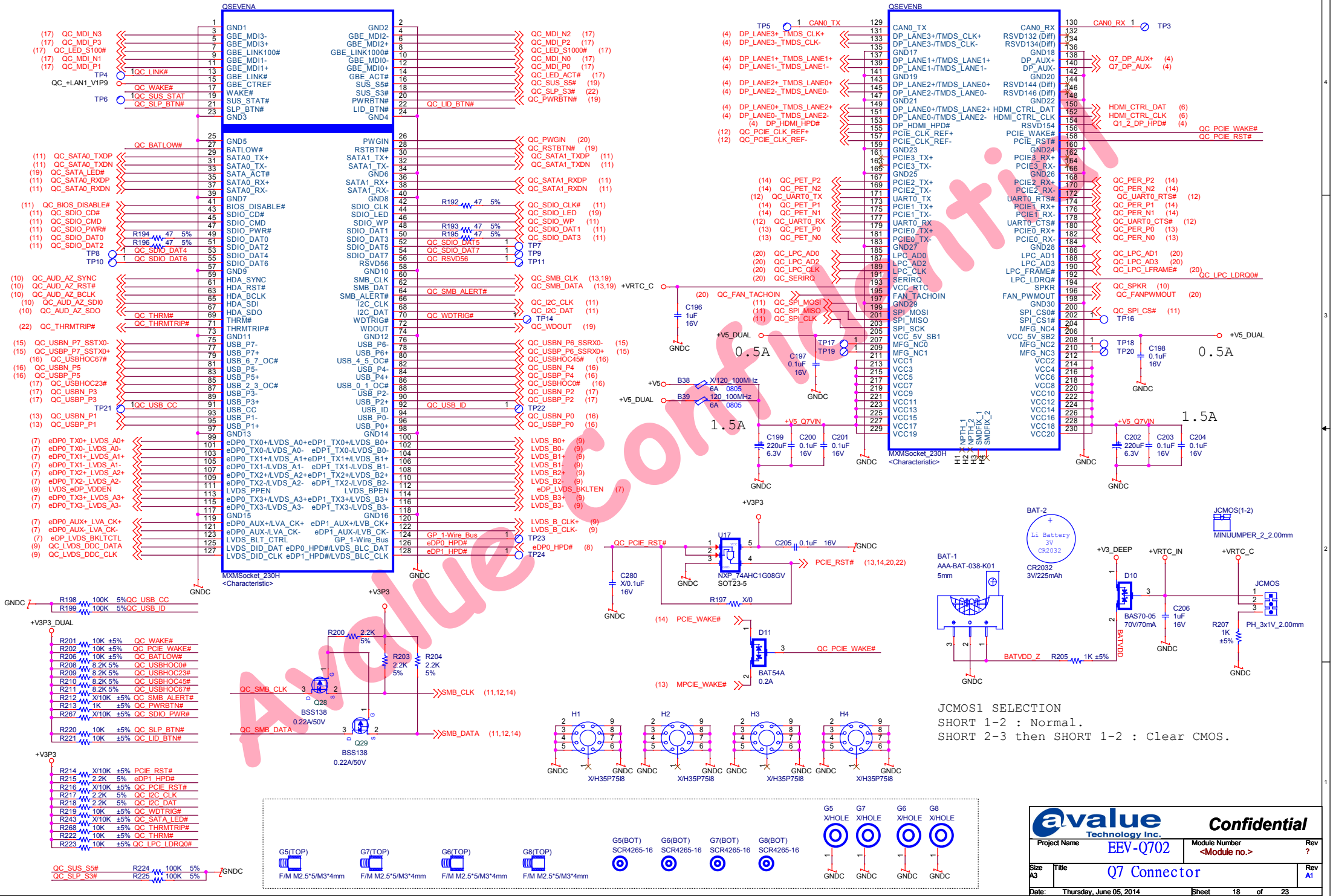
Project Name EEV-Q702		Module Number <Module no.>	Rev ?
Size A2	Title USB 2.0 x 2 with RJ45		Rev A1
Date: Thursday, June 05, 2014		Sheet 17 of 23	

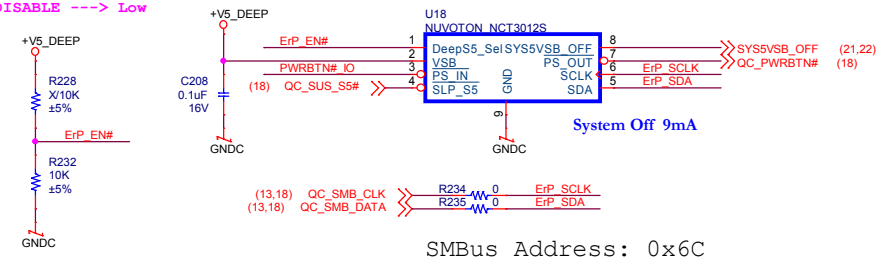
EEV-Q702 design follow QsevenR Specification 2.0



Erp

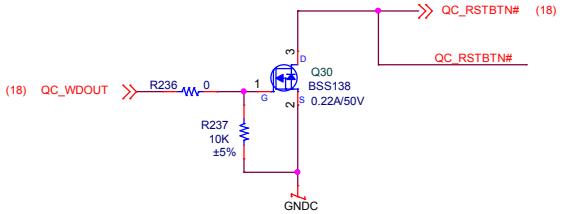
ErP_ENABLE --> Hi
ErP_DISABLE ---> Low

5mA

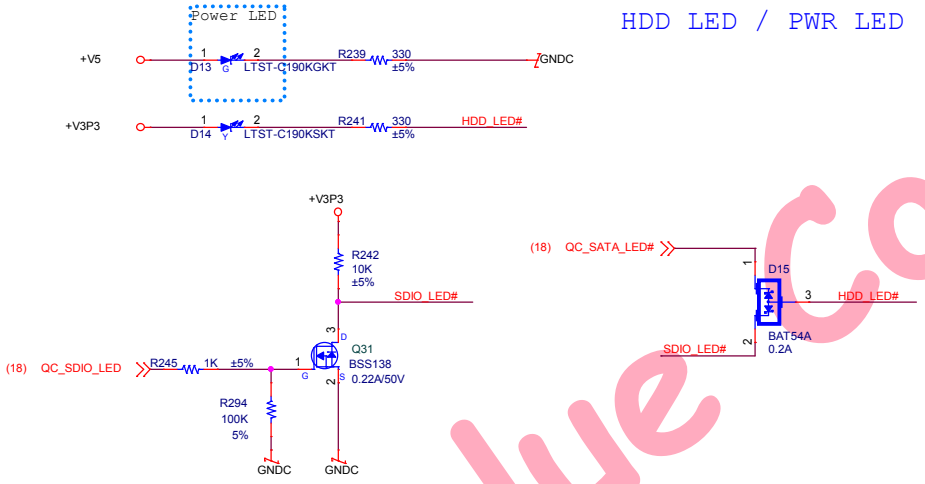


SMBus Address: 0x6C

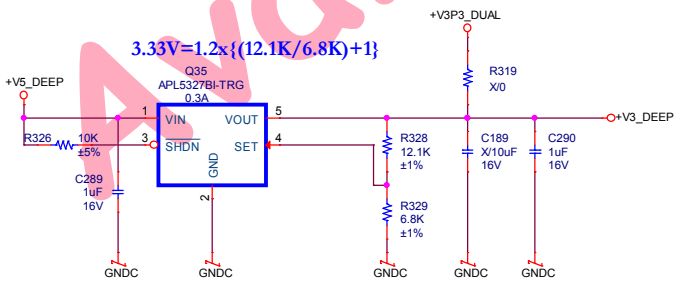
WDT



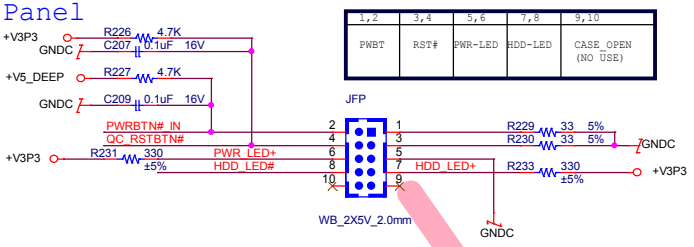
HDD LED / PWR LED



A01 -> A1



Front Panel

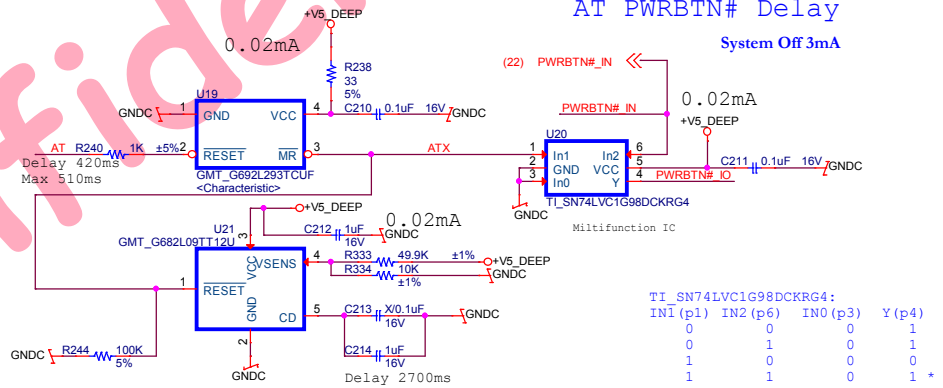


AT / ATX MODE HW Strap

SHORT1-2:AT MODE (default) or
OPEN 1-2:ATX MODE

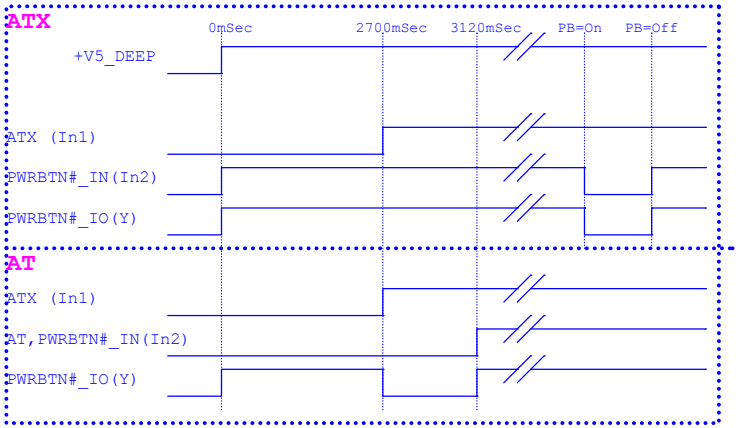
AT PWRBTN# Delay

System Off 3mA



TI_SN74LVC1G98DCKRG4:

IN1(p1)	IN2(p6)	IN0(p3)	Y(p4)
0	0	0	1
0	1	0	1
1	0	0	0
1	1	0	1 *



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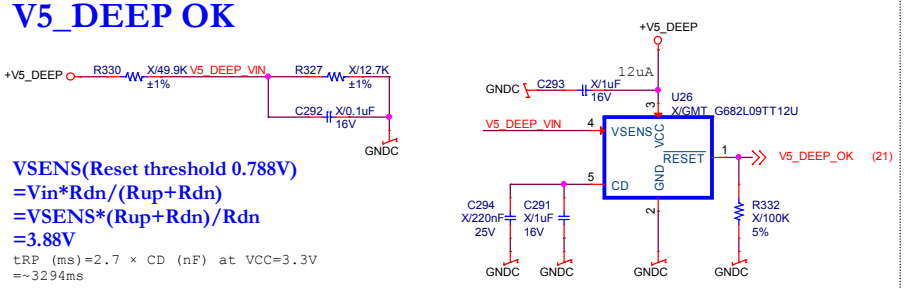
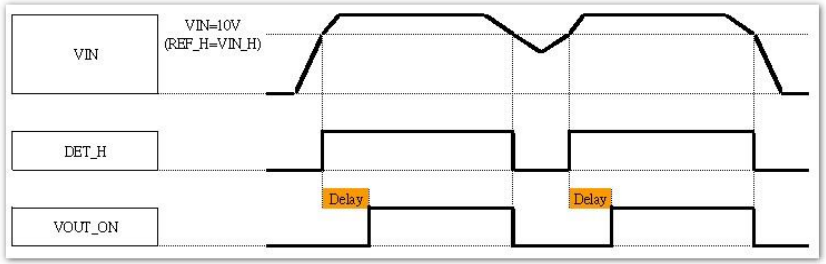
Project Name: EEV-Q702	Module Number: <Module no.>	Rev: ?	
Size: A3	Title: ErP / Front Panel	Rev: A1	
Date: Thursday, June 05, 2014	Sheet 19 of 23		

V5_DEEP OK

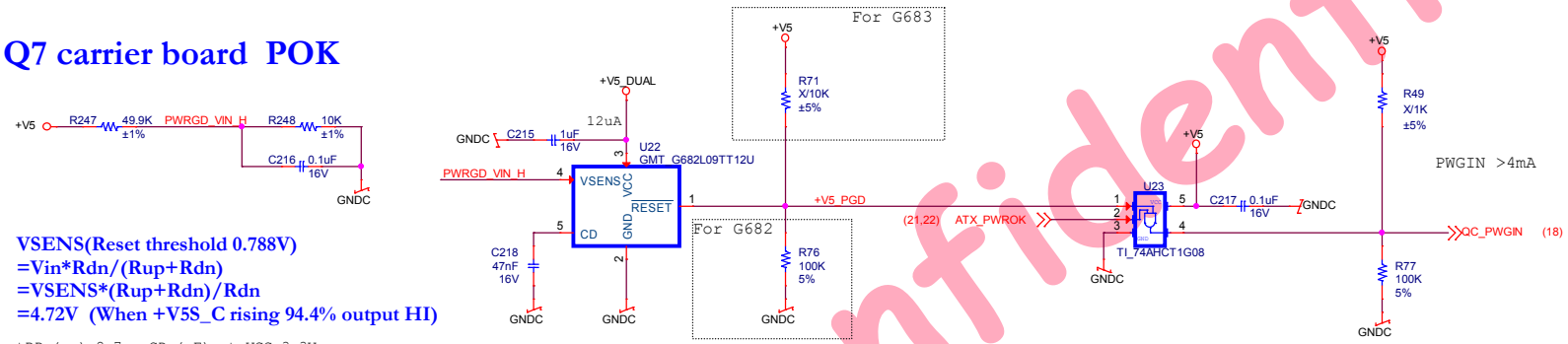


VSENS(Reset threshold 0.788V)
=Vin*Rdn/(Rup+Rdn)
=VSENS*(Rup+Rdn)/Rdn
=3.88V

tRP (ms)=2.7 × CD (nF) at VCC=3.3V
=~3294ms



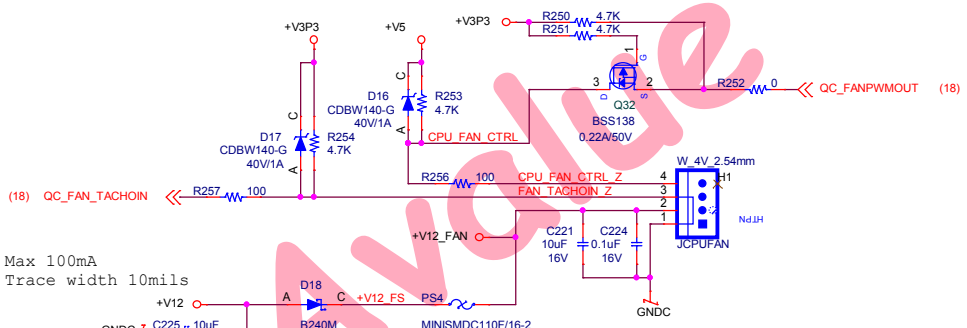
Q7 carrier board POK



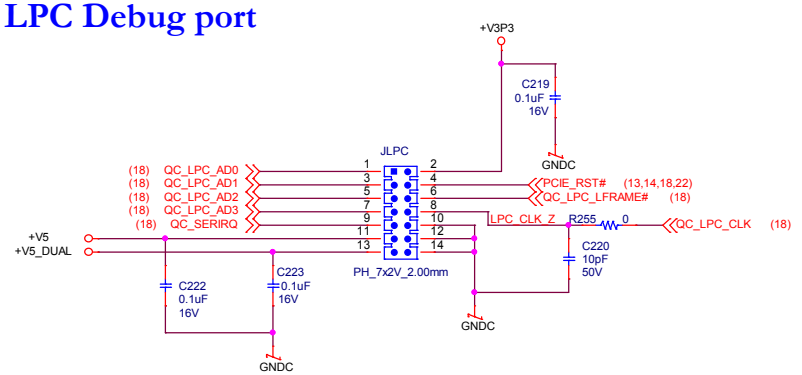
VSENS(Reset threshold 0.788V)
=Vin*Rdn/(Rup+Rdn)
=VSENS*(Rup+Rdn)/Rdn
=4.72V (When +V5S_C rising 94.4% output HI)

tRP (ms)=2.7 × CD (nF) at VCC=3.3V
=~127ms

CPU Fan

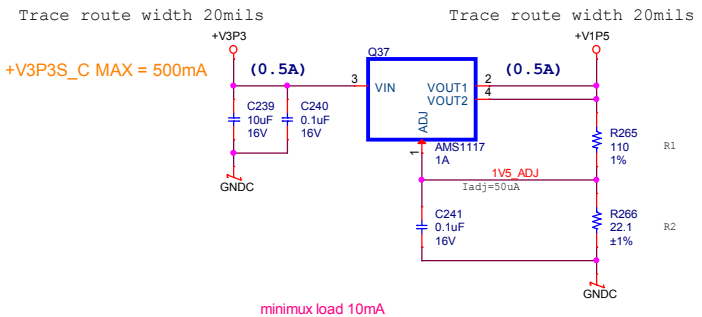


LPC Debug port



avalue Technology Inc.	Confidential	
Project Name: EEV-Q702	Module Number: <Module no.>	Rev: ?
Size: A3	Title: PWR OK / FAN / LPC	Rev: A1
Date: Thursday, June 05, 2014	Sheet 20 of 23	

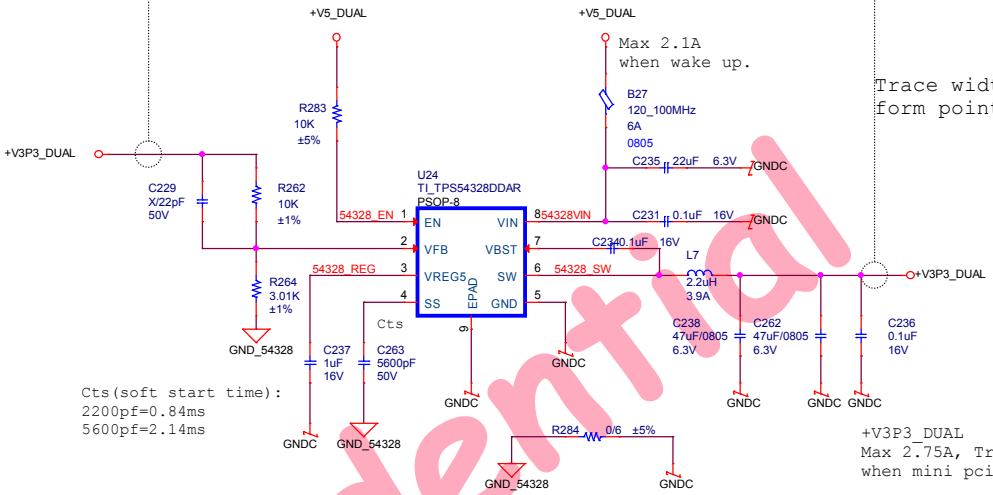
+V1P5 output



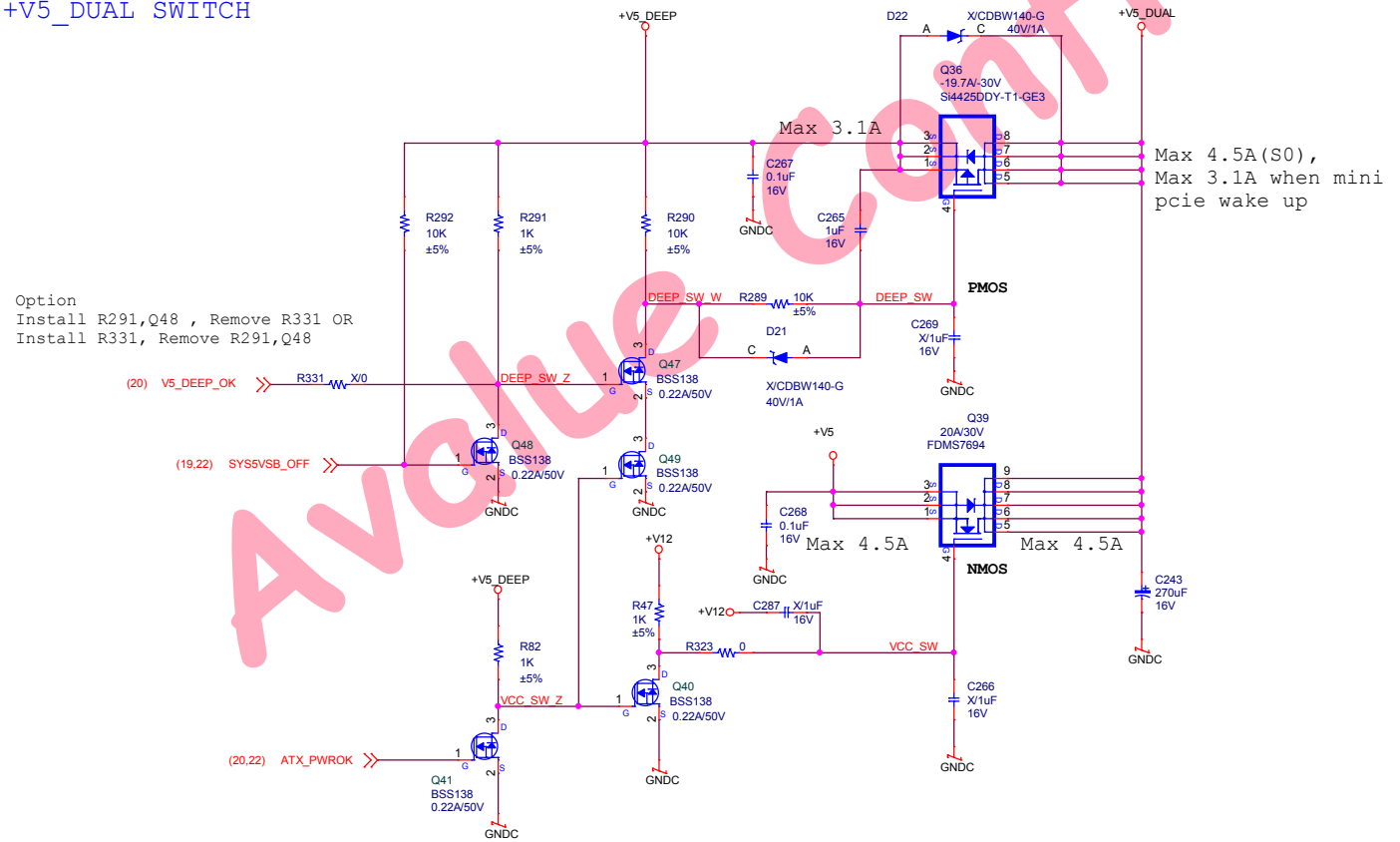
minimux load 10mA
VOUT = VREF (1+ R2/R1)+IADJR2
=1.25 * [1 + (Rd / Ru)]=+1.502 V

LDO:VCC3P3 to VCC1P5 - 500mA

+V3P3_DUAL output



+V5_DUAL SWITCH



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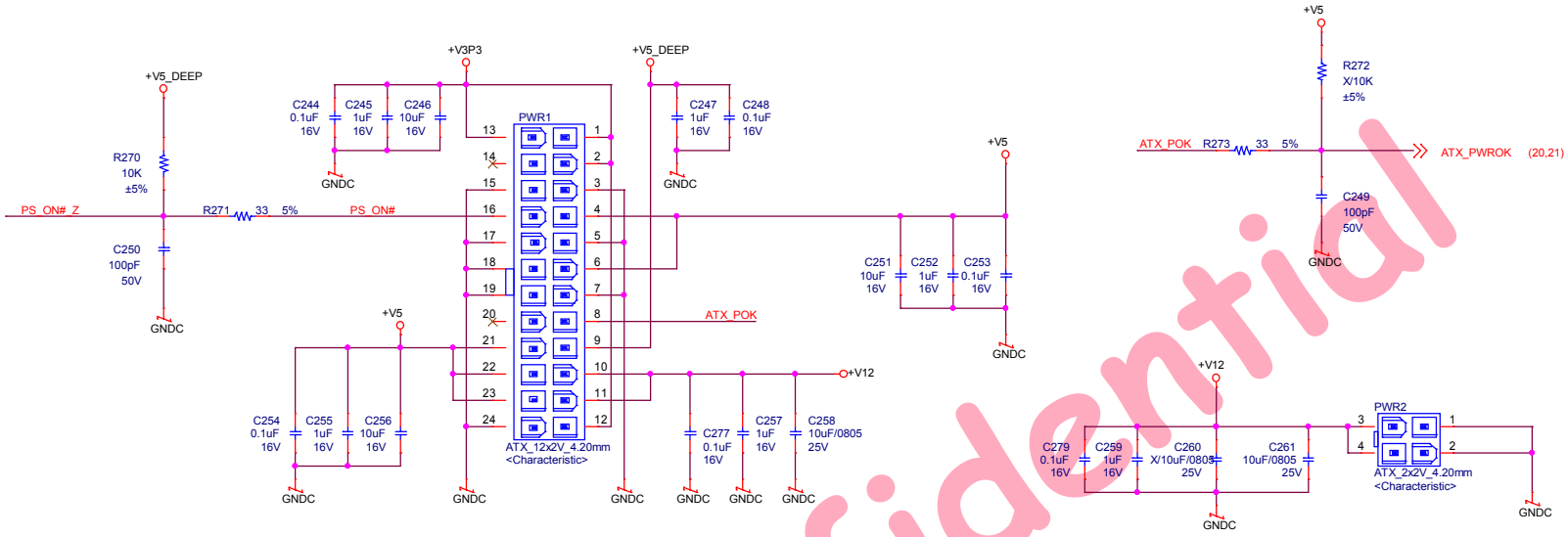
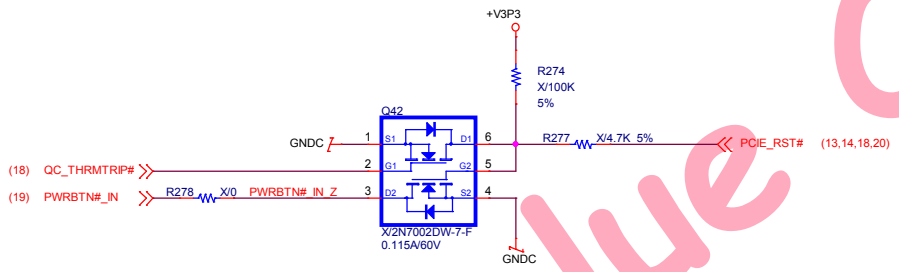
Project Name: EEV-Q702	Module Number: <Module no.>	Rev: ?
Size: A3	Title: +V5_DUAL/+V3P3_DUAL/+V1P5	Rev: A1
Date: Thursday, June 05, 2014	Sheet 21 of 23	

ATX Power IN

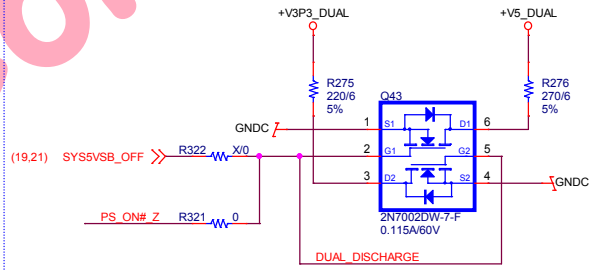
+V5 max 12.5A
+V12 max 4A
+V3P3 max 6A
+V5_DEEP max 3.1A



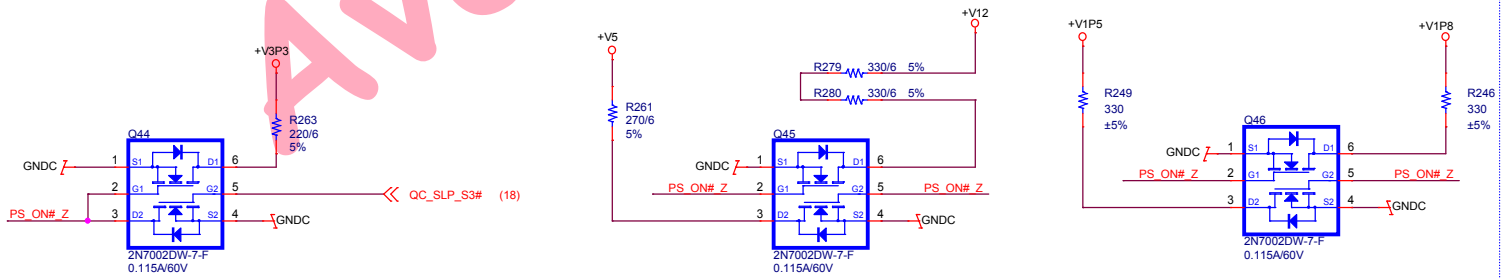
If 'THRMTRIP#' goes active the system immediately transitions to the S5 State



VCC_DUAL discharge



VCC discharge



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